

ELEC301

Lab 4: Hierarchical Schematic Design

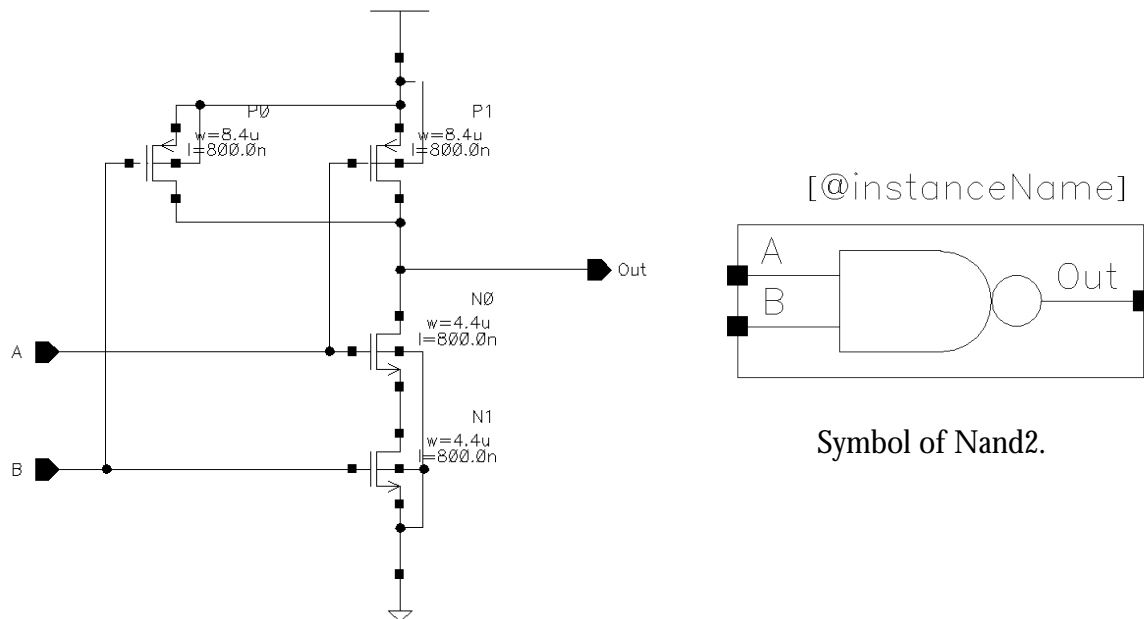
Revision: 2.0
Date: August 98

Objective

- Build schematic of a 2 input NAND gate.
- Understanding hierarchy concept.

Building of a 2 input NAND gate

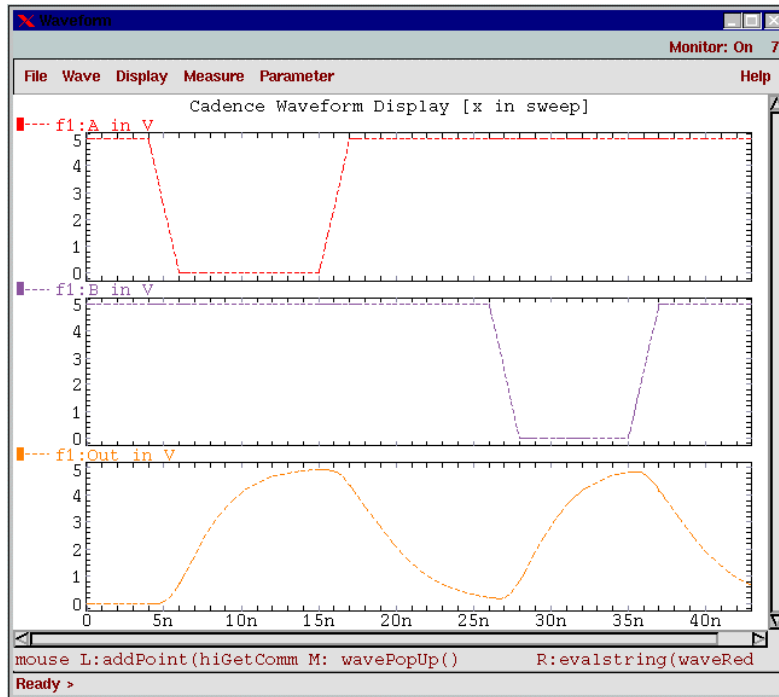
Step 1. Repeat the schematic and the symbol drawing procedures in lab 3 for the 2 input Nand gate (cell name *nand2*). Here are the details,



Schematic of Nand2.

Step 2. Repeat the netlist and circuit simulation procedures in lab 3 for the 2 input Nand gate. Remember to edit the corresponding control file.

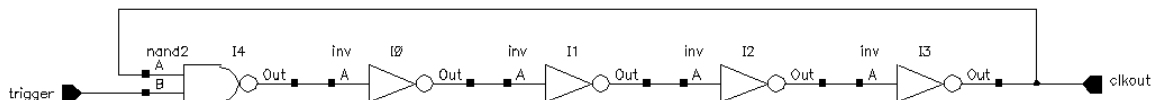
2.1. Measure td_f , td_r of the Nand gate.



Hierarchy design

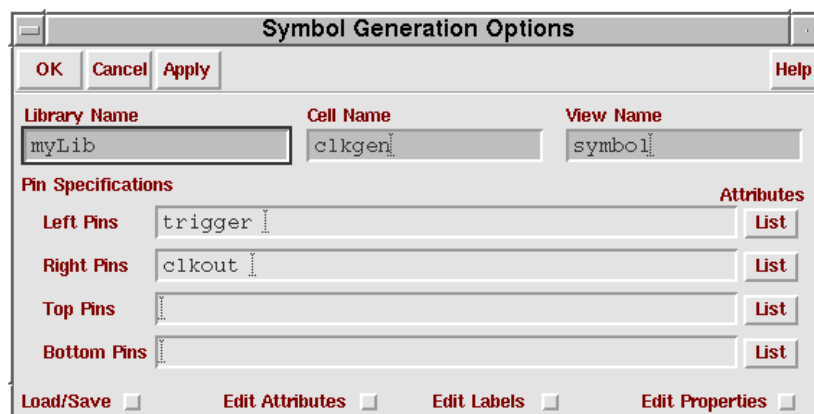
Hierarchy is represented in schematics by referencing the lower level cell with instances of symbols representing those cells. There is no limit on the number of levels of hierarchy you may have in a schematic. Say, you can simplify your designs by using hierarchy.

Step 3. Create the new schematic *clkgen* which containing *inv* and *nand2* you did before. Here are the details,



3.1. Generate symbol cellview automatically.

- Click on **Design -> Create Cellview -> From Cellview**. And press **OK**.

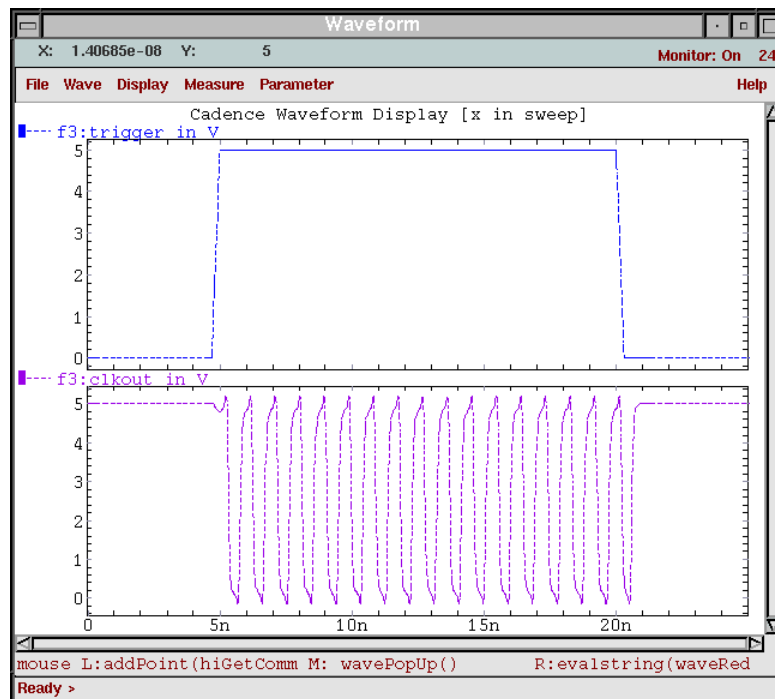


- Then the Symbol Generation Options form appears. The options are used to control how the generated symbol should look like. Leave the default as is and press **OK** again.
- The symbol cellview will be generated as shown,



Step 4. Repeat the simulation process as the same above for your clkgen design.

- Because of weak fanout (output driving capability). The capacitive loading on signal **clkout** is not required. i.e. no capacitor statement for the output pin in **control** file. It applies to **clkout** only.
- The results should something like this

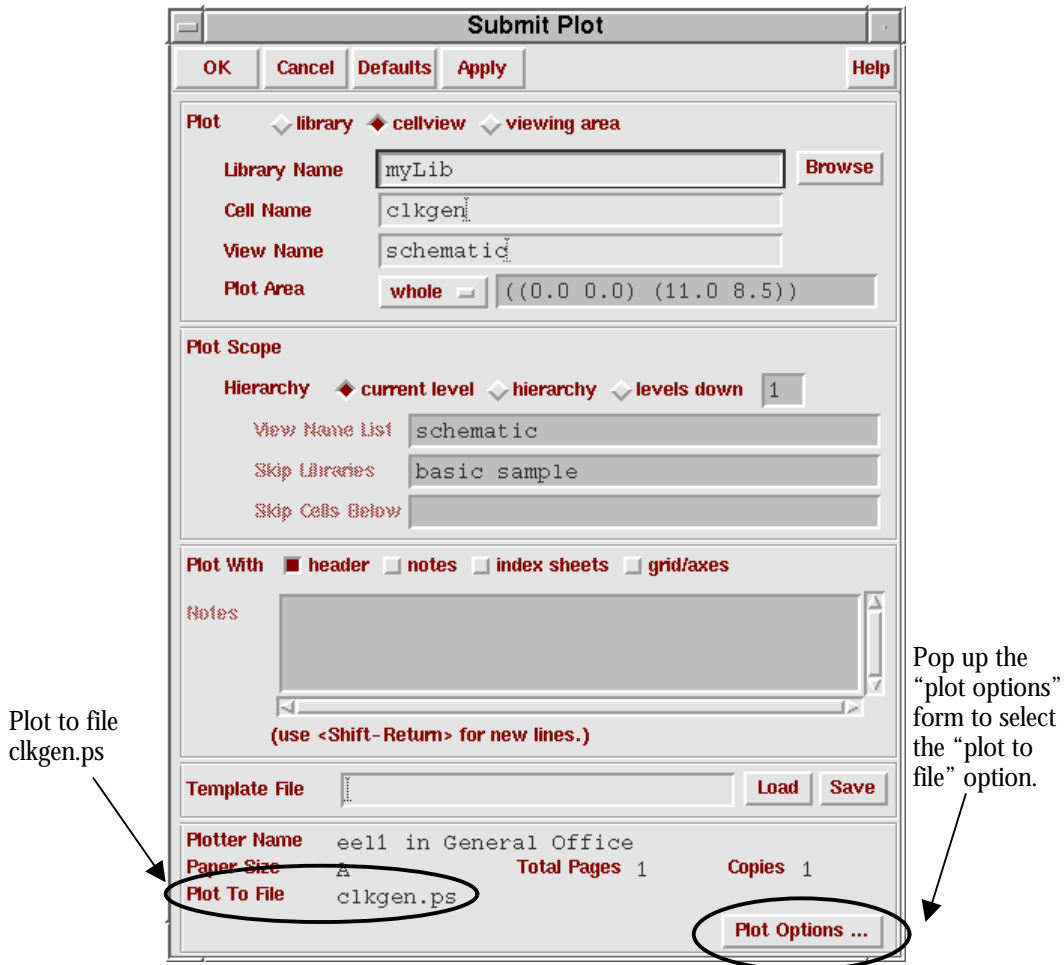


- 4.1. Measure the period of the oscillating signal and calculate the frequency of the periodic signal.

Making hardcopy of schematic

Step 5. Click on **Design - Plot - Submit**.

- Click on Plot Options to set the where the plot should send to.



MAKE SURE enable the option of *Plot to File* then Click on OK.

End of Lab

Useful Hints

1. Using pulse voltage source may help in some cases.

- Here is the example show that the same waveform (generated by pwl) can be reproduced by pulse source. The only different is the entire pulse repeats with a period.

```
vin [#IN] 0 pulse(0 5 5n 2n 2n 7n 20n)
```

