

ELEC301

Lab 3: Schematic Entry and Simulation

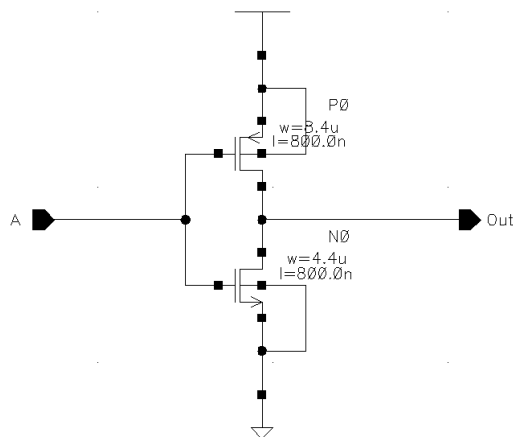
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Objective

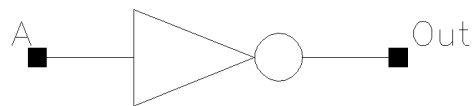
- To learn Cadence schematic editor – Composer.
- Build schematic of an inverter.
- To learn design flow of circuit simulation.
- To obtain the performance of the design by running Spectre on the schematic cellviews.

Introduction to a inverter

Now we are ready to begin useful design work with Cadence. The details of the first step in designing integrated circuit of *inverter* are as follow.



Schematic of an inverter.



Symbol of an inverter.

A	Out
1	0
0	1

Functionality table.

First of all, you will create the schematic by assembling the following elements in the Composer design window.

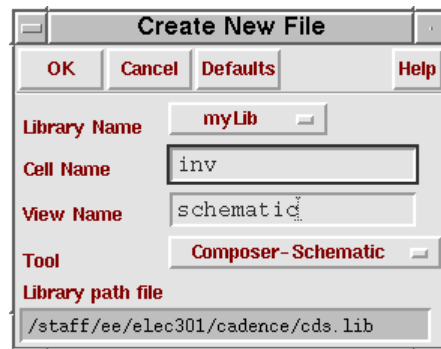
- Sized pmos and nmos transistor components (i.e. 8.4um and 0.8um)
- I/O pin (A and Out)
- Power and Gnd symbol (vdd and gnd)
- Inter-connected wires

Creating a New Schematic Cellview

This tutorial assumes that you have a ~/cadence directory and a library already setup (see lab2). If you do not, you need to go through Lab 2.

Step 1. Starting Cadence under directory ~/cadence.

1.1. In the *Library Manager*, click on **File – New - Cellview**, the form appears,



1.2. In the form enter these values as the same above, then click on **OK**

- A schematic cellview window opens displaying an empty schematic.

Adding a Sheet Border to the Schematic

Step 2. In the schematic window, select **Sheet - Edit Size**.

2.1. Click on **OK** in the Change Sheet Border Size form

- A-size sheet border is added to your schematic.

2.2. To fill in the fields in the title box. Click on **Sheet - Edit Title**

- You may drop down any information in the sheet. For example, you name and schematic name, etc.

Adding Component Instances to the Schematic



Step 3. Getting *pmos4* by Fix Menu

- From the schematic window fixed menu (Left side of Schematic window), select the **Component** bottom.

- An Add component Form shows up, enter the values as below¹.

3.1. Move the cursor onto the schematic window.

- Note that a ghost image of a transistor moves with the cursor within the schematic window. This is referred to as dragging.

3.2. Place the *pmos4* in your schematic by clicking *left mouse button*.

- Press *ESC* to cancels the current active command.

3.3. Using the *Browser* to select Component

- Click fixed menu *Component* again.
- In the form, click on ***Browse***.

The Library browser will be displayed if it is not currently displayed. The ***Add Component*** form can now receive input from the *Browser*.

3.4. Click on the *mosisTechLib* library in *Browser*. You can see few cells appear.

3.5. Click on the *nmos4*.

3.6. Point to the schematic cellview for one of *nmos4* and place it. You may refer to the figure shown in page 1.

¹ You could enter the corresponding parameters in the width/length field when adding the instance. However, in the mean time, just leave it as is because you will be instructed to use another method to fill in the parameters.

Adding Pins to the Schematic



Step 4. From the schematic window fixed menu, select the **Pin** command.

- In the form, enter the pin names separated by spaces:

4.1. Move the cursor into the schematic window and notice that pin shape is now being dragged.

4.2. Point at the location for the input pin A.

- Pin A is added to your schematic, and you can see A has been removed from the Add Pin form.

4.3. In the Add pin form, change the Direction to **output**.

- Place pin *Out*

Add Power and ground symbol

Step 5. Click on *Add component* fixed menu.

- Specify the following on the form

- Be reminded that *vdd* has to be lower case.
- Point to the location for one of *vdd symbol* and place it.

5.1. Add ground symbol by the same procedure shows above.

- Specify cell name *gnd* for ground symbol in *add component* form and place it.
- Be reminded that *gnd* has to be lower case.

Adding Wires to the Schematic



Step 6. Select fixed menu **Wire (narrow)** command

6.1. Move the cursor back into the schematic window. You will see three cursor in the window : arrow, square and Diamond shaped.

6.2. Point at a starting point for a wire and use the left mouse button to begin the wire.

- Refer to figure shown on page 1.

6.3. Enter the next point of the wire as follow:

- Move the mouse so the diamond cursor is at the endpoint for your wire.
- Press the keyboard key **s**.
- The wire is completed to the diamond cursor location.

6.4. There have some options are available when you activating wire command. Press "F3" on the keyboard to bring up option form. Try to make some change and see what effect.

6.5. Add the remaining wires of your inverter schematic using the methods described above.

Modify Transistor sizes (edit properties)



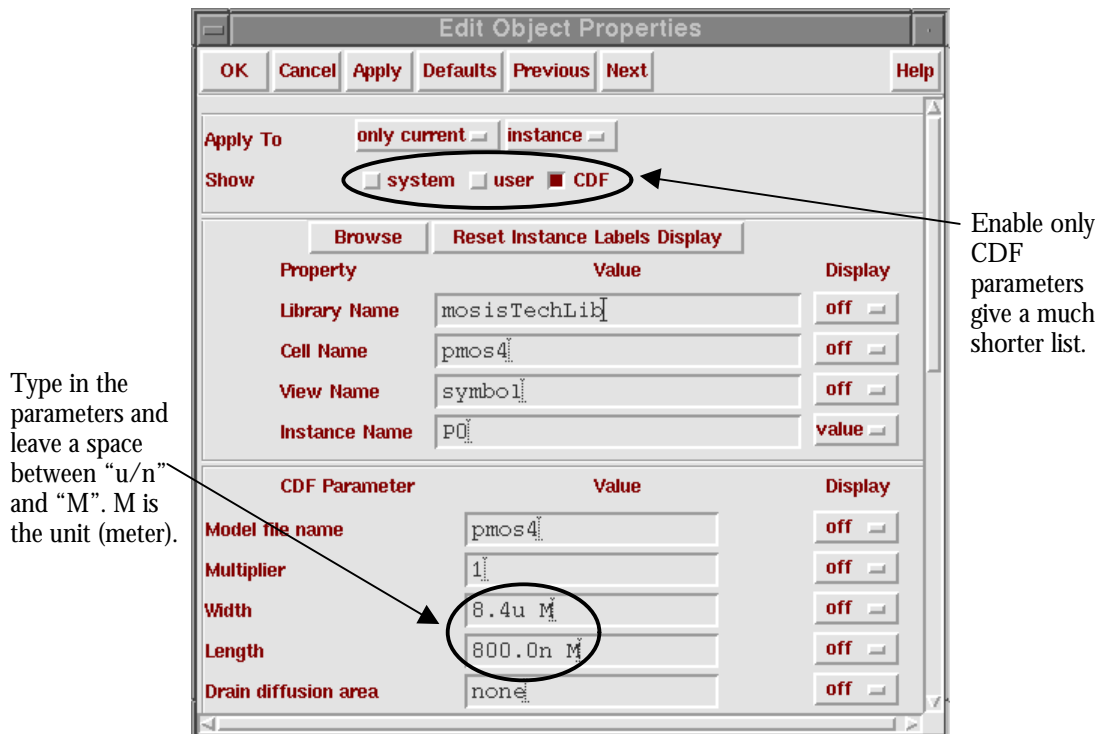
6.6. Set the correct channel length and width of the device

- Select *pmos4* transistor symbol by clicking it on the schematic window.
- Then click on fix menu **properties**.
- *Edit Object Properties* form appears (refer to the figure in the next page), modify the Width (channel width, w) and Length (channel length, l) to *8.4u* and *0.8u* respectively.
- Enable only the **CDF** parameters button.
- The Length will automatically changed to Engineering notation².
- Click **OK**

² The left most digit of the number is non-zero and the exponent is multiple of 3.

6.7. Modify the channel width and channel length of the *nmos4* to $4.4u$ and $0.8u$ by same procedure.

- Deselect *pmos4* by clicking on schematic background.
- Modify the properties of the *nmos4* using the procedure above.



Checking the Schematic

Step 7. Click on *Check - Current Cellview*

- Refer to Appendix A if error exist in the schematic. Otherwise, jump to step 8.

Creating a Symbol cellview

Step 8. Create symbol cellview by using Library Manager.

- 8.1. Open *Library Manager*. You should know how to open it.
- 8.2. Expand the library *myLib* in library browser and pointing to cell **inv**.
- 8.3. In the third column (view), hold down the middle bottom and select **New**.
- 8.4. Fill in the View name **symbol** in the form appears then click on **OK**.

- A symbol cellview appear in library browser.
- A symbol cellview window opens and displaying an empty symbol.

8.5. Draw the symbol of inverter using by pull down the menu of

- *Add - Shape - Line* and *Add - Shape - Circle*.
- Remember you can use *option form* for those commands.

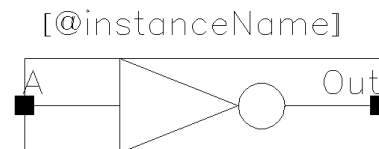
8.6. Adding pin and pin name by using the *Add - Pin* command

8.7. Adding the Label [*@instanceName*] and *inv* by using *Add - Label* command

8.8. Adding the Selection Box by using *Add - Selection Box* command

8.9. Last bring the symbol to origin by using the *Edit - Origin* command and pointing to the pin A.

The diagram would be like this:



Well done. you just finish the inverter design including schematic and symbol cell view. In the following section, you will be introduced the circuit simulation and the performance estimation of the design.

Spectre Circuit Simulator

Spectre is a modern circuit simulator that uses direct methods to simulate analog and digital circuits at the differential equation level. The program is similar in function and application to SPICE but is not a descendant of SPICE. Spectre uses the same basic algorithms found in SPICE, but every algorithm is newly implemented.

Initialization

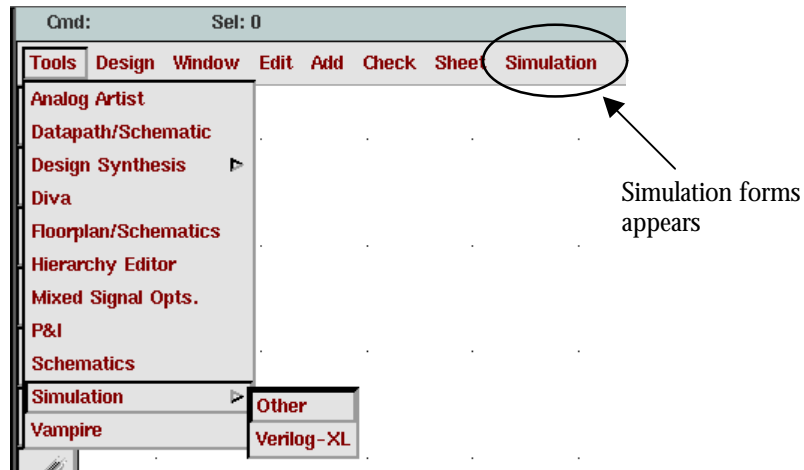
Before you can simulate the design, you must first set up the simulation environment. This involves identifying the circuit you want to simulate, identifying a directory for containing the simulation date (i.e., a Simulation Run Directory) and selecting a simulator.

Step 9. From *Library Browser*, open the **inv** schematic from **myLib** library.

- Make sure there have no errors in the schematic.

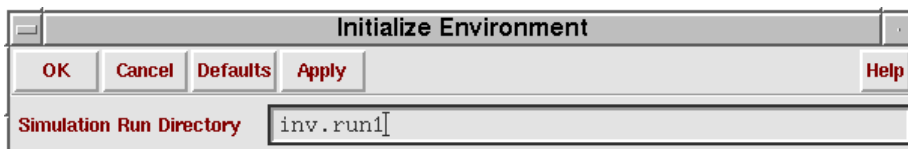
Step 10. In **Schematic window**, Click on **Tools - Simulation - Other**

This command changes the banner menu to include the “Simulation” menu.



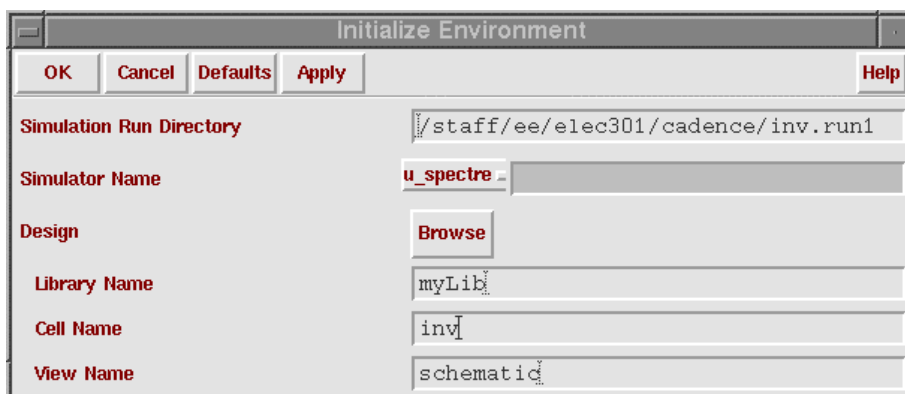
10.1. Click on menu *Simulation - Initialize*

The following Initialize form will appear,



- Change Simulation Run Directory to **inv.run1**, then click on **OK**.
- A second Initialize Environment form opens since the run directory does not exist. All of the files associated with this simulation will reside in this directory.

10.2. Clicking on the *Simulator Name* popup menu and selecting *u_spectre*.



10.3. Click on **OK**.

- The *run directory* (*inv.run1*) for your simulation had created. After this process, some files has also be created in *run directory*. Check to see what kind of files in there.

Understanding the Simulation Input File

Before you can simulate, you must generate a input file for your design.

- Here is the input file named *control* in your run directory. You need to modify this file as shown below using text editor. e.g. vi or pico.

```

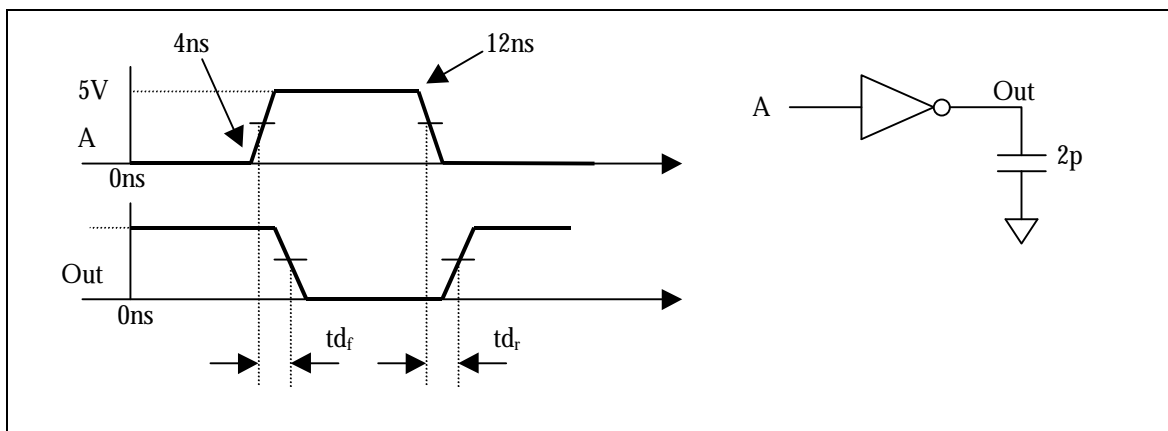
simulator lang=spice
.trans .01n 20n
vdd [#vdd!] 0 dc 5
va [#A] 0 pwl (0n 0 4n 0 6n 5 12n 5 14n 0)
c1 [#Out] 0 2p
save [#A] [#Out]
[!modelFile]
[!netlist]
.end

```

Annotations:

- Transient analysis for 15ns with .01ns time step (points to `.trans .01n 20n`)
- Voltage Source (points to `vdd` and `va`)
- Piecewise Linear (pwl) input voltage source for pin A (points to `pwl (0n 0 4n 0 6n 5 12n 5 14n 0)`)
- Capacitive load for pin *Out* (Be reminded the pin name is case sensitive and should be the same as in schematic.) (points to `c1 [#Out] 0 2p`)
- Cadence defaults (points to `[!modelFile]` and `[!netlist]`)
- Store only those signals to the waveform file (points to `save [#A] [#Out]`)

- We will run simulation with the following waveforms (according to file *control*), applying at the inputs of the inverter.

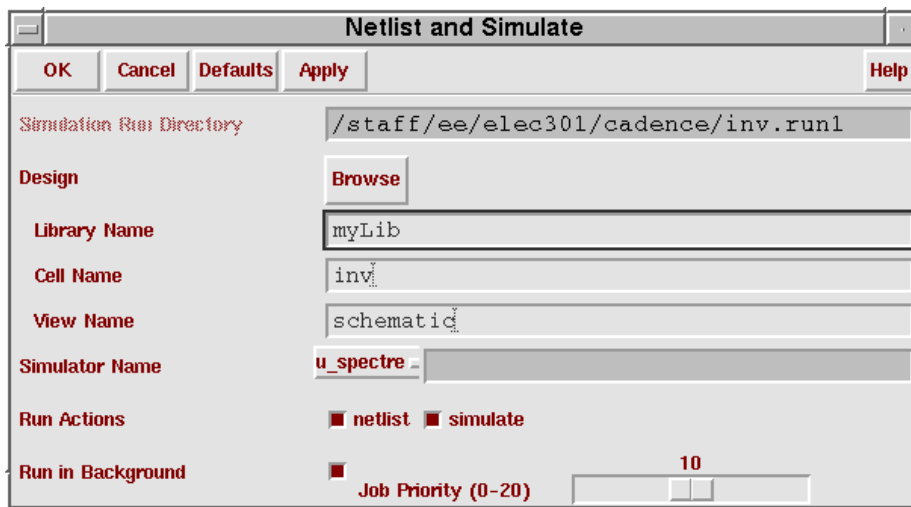


Creating Netlist and Running the Simulation

Since you have prepared a input file, you can now run the simulation. You will be running simulation in the background.

Step 11. In **schematic** window, select *Simulation - Netlist/Simulate*

Netlist and **Simulate** window appears,



- Leave all default and click on **OK**.
Then the netlist will be first generated (file name **netlist** under your run directory *inv.run1*, check for this) and then the simulation runs.

Step 12. Since this job is run in the background, the dialog box will be appeared after simulation completed.

- Check the *CIW* window to ensure the simulation completed without errors.
- The message area should state "Simulation completed successfully." If the simulation did not complete successfully, check the error messages in the *CIW* to determine the cause of failure.

Note: A common cause of failure could be that you forgot to run a Check on the schematic before saving the design. Failure to execute this step will result in the schematic not getting extracted, therefore, the simulation can not run.

Viewing the Spectre Output File

Check to see if there have any run time error during simulation.

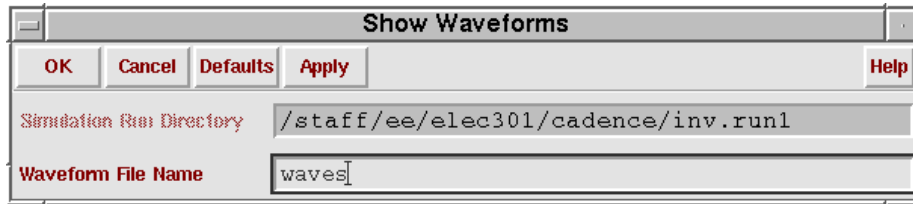
Step 13. Select *Simulation - Show Outputs - Show Output*

- The simulator output file is displayed in a window.
- You can process next step if there have no error found.

Viewing the Output Waveform

Step 14. In *schematic* window, click *Simulation - Show Waveform*

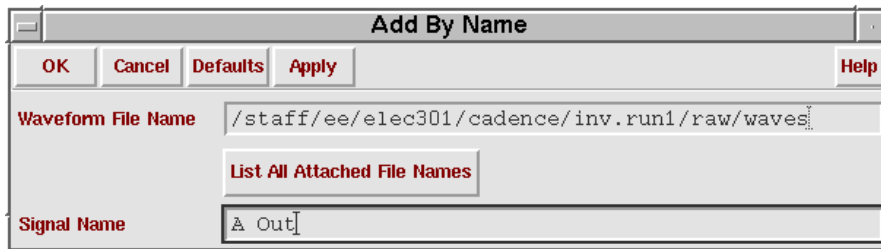
A dialog box prompts you for the resulting waveform file. Check to see the *run directory* name is corrected. The filename *waves* should not be changed.



- Click on **OK**.

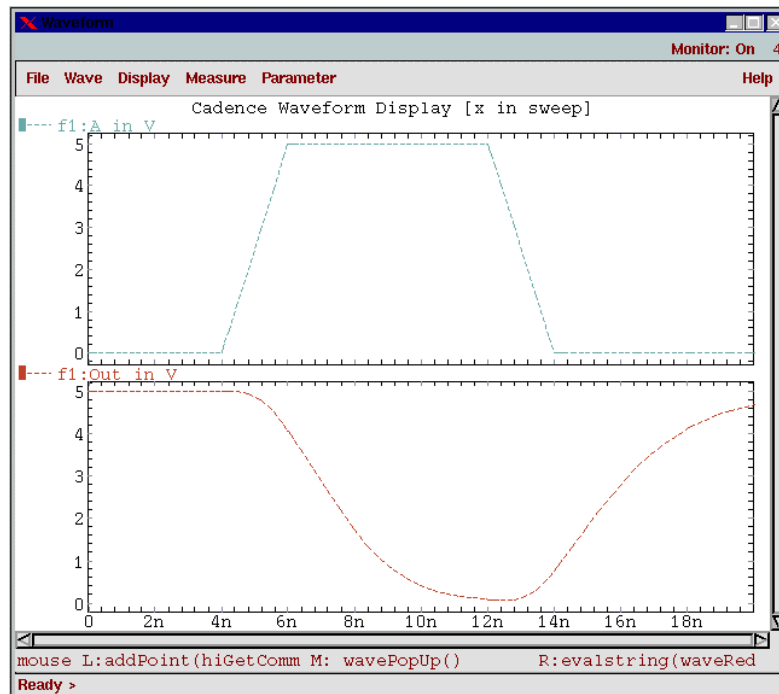
A *waveform window* appears. Jump to next step if there have no error found.

14.1 In waveform window, click on **Wave - Add by name**



- Type Signal Name **A Out** as above (or signal names you want to see).
- Click on **OK**.

In waveform window, 2 waveforms display (one for each signal) as below. Notes that **Y-axis** is voltage level of signal, **X-axis** is time.



- Spend some time using the different command in the Waveform window. e.g. Zoom in, Zoom Out in menu **Display**.

Obtaining the Gate Delay

The simulation for this lab is **transient analysis**, using to measure the **rising and falling gate-delay** (represented by td_r and td_f respectively).

td_r is defined as delay from “input falling to VDD/2” to “output rising to VDD/2”

td_f is defined as delay from “input rising to VDD/2” to “output falling to VDD/2”

Step 15. To measure td_r

- In waveform window, click on *Measure - Set Anchor*
- Move cursor along **falling slope of A waveform** around **Y=2.5v** and click left mouse button, an cross will stay on that location. Then move cursor along **rising slope of Out waveform** until **Y=2.5v**, record **dx (=td_r)**

15.1. To measure td_f

- Click on *Measure - Set anchor* again.

Move cursor along **rising slope of A waveform** around **Y=2.5v** and click left mouse button, an cross will stay on that location. Then move cursor along **falling slope of Out waveform** until **Y=2.5v**, record **dx (=td_f)**

- Record the rise (td_r) and fall (td_f) time delay of your design and report the result to your lab TA.

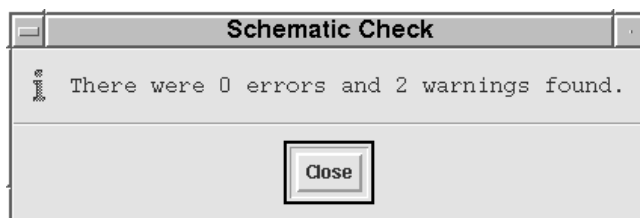
15.2. In waveform window. Select *Display - Close Window...*

End of Lab

Appendix: Trouble Shooting

In many cases, don't think that warnings can be ignored. Try to fix all the warning before you proceed to next step, it will surely save you a lot of time. (This is especially true when you're doing your project.)

A.1. *Close* the Dialog box.



- View the error list in the CIW.

A.2. Select *Check - Find Marker*

- In the Find Marker form, toggle *Zoom To Markers* on
- Click on *Apply* in the Find Marker form.

Make sure you are not missing the warnings.

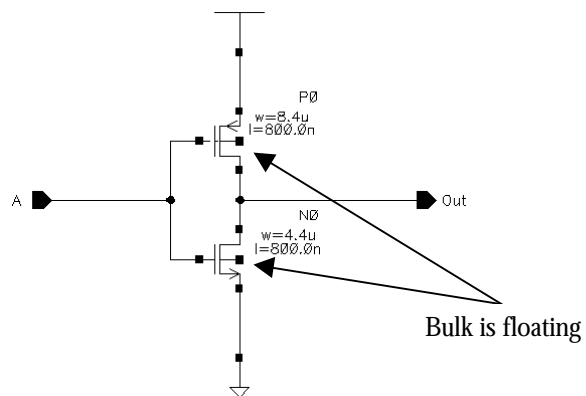
Enable the "Zoom To Markers" option and adjust the scale when necessary.

The marker for the first warning or error is centered in the schematic entry window. A text window appears with the explanation for the marker.

A.3. Correct the problem. In this example, it's due to two floating connection of the bulk of the two transistors.

A.4. In the Find Marker form, click on **Next**.

A.5. Repeat the procedure until a number of problems have been corrected.



A.6. **Check and Save** the schematic after a number of problems have been corrected, as one mistake in the schematic may cause multiple problems and rechecking the schematic may clear a number of problems.

A.7. Continue debugging the schematic in this manner until all problems have been corrected and schematic check passes with no warnings or errors in the CIW.