Planar Integration of E/D-Mode AlGaN/GaN HEMTs Using Fluoride-Based Plasma Treatment

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Abstract—A planar-fabrication technology for integrating enhancement/depletion (E/D)-mode AlGaN/GaN high-electron mobility transistors (HEMTs) has been developed. The technology relies heavily on CF₄ plasma treatment, which is used in two separate steps to achieve two objectives: 1) active device isolation and 2) threshold-voltage control for the enhancement-mode HEMT formation. Using the planar process, depletion- and enhancement-mode AlGaN/GaN HEMTs are integrated on the same chip, and a direct-coupled FET logic inverter is demonstrated. Compared with the devices fabricated by a standard mesa-etching technique, the HEMTs by a planar process have comparable dc and RF characteristics with no obvious difference in the device isolation. The device isolation by a plasma treatment remains the same after 400 °C annealing, indicating a good thermal stability. At a supply voltage ($V_{DD}$) of 3.3 V, the E/D-mode inverters show an output swing of 2.85 V, with the logic-low and logic-high noise margins at 0.34 and 1.47 V, respectively.

Index Terms—AlGaN/GaN, enhancement/depletion (E/D)-mode high-electron mobility transistors (HEMT), fluoride-based plasma treatment, planar process.

I. INTRODUCTION

Owing to the excellent thermal and chemical stability associated with the wide bandgap semiconductor materials, AlGaN/GaN high-electron mobility transistors (HEMTs) are attracting increasing interests in the integrated circuits (ICs) used in harsh conditions [1]–[3]. Recently, the digital ICs based on the integrated enhancement/depletion (E/D)-mode HEMTs have been demonstrated using a recess gate [4] and fluoride-plasma-treatment techniques [5], both of which used a mesa etching to achieve the active device isolation. To achieve high-density and high-uniformity in the E/D HEMT integration, the three-dimensional mesas impose serious limits to photolithography and interconnects. Thus, a planar process is desired, as seen from the successful development of the commercial GaAs MESFET ICs [6], [7]. Recently, we demonstrated a new technique of fabricating the enhancement-mode (E-mode) AlGaN/GaN HEMTs using a fluoride-based plasma treatment [8]. The incorporation of the fluorine ions in the AlGaN barrier can effectively deplete the electrons in the active channel, giving a strong indication that it could be used for an active isolation as well.

In this letter, the fluoride-based plasma treatment technique is adopted to selectively define the active regions of the HEMTs. The device isolation achieved by this technique is as good as that achieved by the mesa etching. A planar integration for E/D HEMTs is demonstrated without any mesa etching and gate-recess etching. Device isolation and device performance are maintained after annealing at 400 °C, indicating a good thermal stability for the fluorine ions in the AlGaN/GaN heterostructures.

II. DEVICE STRUCTURE AND FABRICATION

The AlGaN/GaN HEMT structure used in this letter is grown on (0001) sapphire substrates in an Aixtron AIX 2000 HT metal-organic chemical deposition (MOCVD) system. The HEMT structure consists of a low-temperature GaN nucleation layer, a 2.5-μm thick unintentionally doped GaN buffer layer, and an AlGaN barrier layer with a nominal 30% Al composition. The barrier layer is composed of a 3-nm undoped spacer, a 21-nm carrier supplier layer doped at 2 × 10¹⁸ cm⁻³, and a 2-nm undoped cap layer. Room-temperature hall measurements of the structure yield an electron sheet density of 1.3 × 10¹⁵ cm⁻² and an electron mobility of 950 cm²/Vs.

The integration process flow is illustrated in Fig. 1. At first, the source/drain ohmic contacts of the E/D-mode devices are formed simultaneously by a deposition of e-beam evaporated Ti/Ai/Ni/Au (20 nm/150 nm/50 nm/80 nm) and rapid thermal annealing (RTA) at 850 °C for 30 s, as shown in Fig. 1(a). Secondly, the active regions for both E/D-mode devices are patterned by a photolithography, which is followed by the CF₄ plasma treatment in a reactive ion etching (RIE) system. The plasma power is 300 W, and the treatment time is 100 s. The gas flow is controlled to be 150 sccm, and the plasma bias is set to be 0 V. The isolation regions are the locations where a large amount of F⁻ ions are incorporated in the AlGaN and GaN layers near the surface, and then deplete the two-dimensional electron gas (2DEG) in the channel, as shown in Fig. 1(b). The D-mode HEMTs’ gate electrodes are then patterned by the contact photolithography, which is followed by the e-beam evaporation of Ni/Au (50 nm/300 nm) and liftoff [Fig. 1(c)]. Next, E-mode HEMTs’ gate electrodes and interconnections are defined. Prior to the e-beam evaporation of Ni/Au, the gate regions of the E-mode HEMTs are treated by the CF₄ plasma (which has a negligible etching to AlGaN) at 170 W for 150 s, as shown in Fig. 1(d). This plasma treatment performs the
Fig. 1. Schematics showing the process flow of E/D-mode HEMTs: (a) Ohmic contact. (b) Active region definition by a plasma isolation. (c) D-mode gate formation. (d) E-mode gate definition and plasma treatment. (e) SiN passivation.

function of converting the treated devices from the D-mode to E-mode HEMT [8]. A 200-nm-thick SiN passivation layer is deposited by the plasma enhanced chemical vapor deposition (PECVD), and the probing pads are opened. Then, the sample is annealed at 400 °C for 10 min to repair the plasma-induced damage in the AlGaN barrier and channel of the E-mode HEMTs [Fig. 1(e)]. As a comparison, the D-mode devices are also fabricated on another piece of the sample from the same substrate by the standard process, in which inductively coupled plasma reactive ion etching (ICP-RIE) is used to define the mesa as the active region. For the direct-coupled FET logic (DCFL) inverter shown in this letter, the E-mode HEMT driver is designed with a gate length, gate–source spacing, gate–drain spacing, and gate width of 1.5, 1.5, 1.5, and 50 µm, respectively; the D-mode HEMT load is designed with a gate length, gate–source spacing, gate–drain spacing, and gate width of 4, 3, 3, and 8 µm, yielding a ratio $\beta = (W_E/L_E)/(W_D/L_D)$ of 16.7. Discrete E-mode and D-mode HEMTs with 1.5 × 100 µm gate dimension are fabricated for characterizations.

III. Device and Circuit Characteristics

For the E/D-mode HEMTs fabricated by the planar process, the output characteristics are plotted in Fig. 2. The peak current density for D-mode and E-mode HEMTs are about 730 and 190 mA/mm. Fig. 3 shows the dc transfer characteristics

Fig. 2. DC output characteristics of (a) D-HEMT and (b) E-HEMT by a planar process.
comparison between the planar and the standard process. It can be seen that the drain leakage current for the planar process is $\sim 0.3 \, \text{mA/mm}$, reaching the same level as the devices fabricated by the standard mesa etching. The D-mode HEMTs by the planar process have the comparable drain–current and transconductance characteristics [Fig. 3(b)] as the ones by the standard process. Also, we measure the leakage current between two pads $(400 \times 100 \, \mu \text{m}^2)$ with the spacing of 150 $\mu \text{m}$. At the dc bias of 10 V, the leakage current by the planar process is about 38 $\mu \text{A}$, at the same level of the standard mesa-etching sample $(\sim 30 \, \mu \text{A})$. It is proved that, compared with the standard mesa process, the fluoride-based plasma treatment can achieve the same level of the active device isolation, enabling a complete planar-integration process. The E-mode HEMTs exhibit a smaller transconductance $(g_m)$ compared to the D-mode devices, which is due to the incomplete recovery of the plasma-induced damage [8]. The fact that the sample has been through a thermal annealing at 400 $^\circ \text{C}$, it also indicates that a good thermal stability is expected at a temperature at least up to 400 $^\circ \text{C}$. It should be noted that an ion-implantation technique has also been developed for inter-device isolation accomplished by a multiple energy N$^+$ implantation to produce a significant lattice damage throughout the thickness of the GaN buffer layer [9]. Compared to the ion-implantation technique, the CF$_2$ plasma-treatment technique has the advantages of low cost and low damage.

An E/D-mode HEMTs DCFL inverter fabricated by the planar-integration process is characterized. Fig. 4 shows the measured static voltage transfer curve of the inverter at a supply voltage $V_{DD} = 3.3 \, \text{V}$. High- and low-output logic levels $(V_{OH}$ and $V_{OL})$ are 3.3 and 0.45 $\text{V}$, respectively, with the output swing $(V_{OH} - V_{OL})$ of 2.85 $\text{V}$. The dc voltage gain in the linear region is 2.9. By defining the values of $V_{IL}$ and $V_{IH}$ at the unit gain points, the low and high noise margins are 0.34 and 1.47 $\text{V}$. The inverter dc current is also shown in Fig. 4. The leakage current with the E-mode device pinchoff is about $3 \, \mu \text{A}$, which is consistent with the discrete device results.

IV. CONCLUSION

A new planar process for integration AlGaN/GaN E/D HEMTs is demonstrated based on the fluoride-based plasma treatment. Without any dry etching for the mesa formation and gate recess, the plasma treatment can achieve the same isolation results between active devices. The plasma treatment can also be used to convert D-mode HEMTs to E-mode. The E/D-mode DCFL inverter has been demonstrated using this new technique, in which the whole process is conducted on a pure planar surface. This planar-integration technology is expected to be beneficial to the development of the GaN-based large-scale integration (LSI).

REFERENCES


