GaAs Esaki junctions with autocompensated impurities in the $n$ side by metalorganic chemical vapor deposition

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GaAs Esaki junctions were grown at normal growth temperatures above 550 °C by low pressure metalorganic chemical vapor deposition. The $n$ sides of these junctions were heavily doped with silane into the regime that impurities were autocompensated. Consequently, zero-bias tunnel resistance was significantly reduced. We obtained a low zero-bias specific tunnel resistance of $9.6 \times 10^{-5}$ $\Omega \cdot \text{cm}^2$ with an optimized silane flow rate. © 2004 American Institute of Physics.

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GaAs Esaki junction$^1$ has many applications in vertical monolithic integration. It can be used to cascade multijunction solar cells,$^{2,3}$ to integrate a laser diode with a microcooler,$^4$ to fabricate multi-active-region lasers,$^5,6$ and to bury a heterostructure for current confinement.$^7$ For these applications, the GaAs Esaki junctions are required to have low zero-bias tunnel resistances to reduce parasitic joule heating. In order to do so, an intuitive thought is to increase the carrier concentrations of the $n$ and $p$ sides of the junctions to extremely high levels.$^8$ It is well known that the maximum achievable electron concentrations of GaAs grown at temperatures above 500 °C are only around $1-2 \times 10^{19}$ $\text{cm}^{-3}$.$^9,10$ According to theoretical evaluation based on the band-to-band tunneling model,$^1,11$ the concentrations of this level are insufficient to produce Esaki junctions with zero-bias tunnel resistances low enough to support most of the integration applications. Some alternative ways need to be employed to fabricate the tunnel junctions. Low zero-bias tunnel resistances have indeed been achieved from Esaki junctions using low-temperature-grown nonstoichiometric GaAs$^{12}$ or low-temperature-grown (111)- or (110)-oriented GaAs.$^{13}$ These junctions, however, are subject to severe degradation$^{12}$ when the temperatures are raised above 550 °C required for the growth of most device structures. In this letter, GaAs Esaki junctions with autocompensated $n$-side impurities grown by metalorganic chemical vapor deposition (MOCVD) at temperatures above 550 °C are reported. Low zero-bias tunnel resistances were obtained from some junctions, though the electron concentrations are low on the $n$ sides. The lowest zero-bias specific tunnel resistance we achieved is $9.6 \times 10^{-5}$ $\Omega \cdot \text{cm}^2$ which is much lower than the best previously reported result of $1.4 \times 10^{-4}$ $\Omega \cdot \text{cm}^2$ for a GaAs Esaki junction grown at temperatures above 550 °C.$^{12,14,15}$

The GaAs Esaki junctions were grown at 100 mbar in an AIXTRON 200/4 horizontal reactor. The graphite susceptor was heated by lamps, and the samples were rotated at around 50 rpm during growth. Trimethylgallium (TMGa) and arsine were the gallium and arsenic sources, respectively. A 2% diluted silane was used for $n$-type doping while carbon tetrachloride for $p$ type. Each tunnel junction was formed in a single run by first growing an $n$-type GaAs layer at 700 °C on an $n$-type (100)-oriented substrate with an input V/III ratio of 202, and then depositing a $p$-type GaAs at 550 °C with the input V/III ratio of 25. Five such junctions were consecutively grown with the same growth parameters except the silane flow ratio used for doping the $n$ side of each junction. The silane flow ratio was defined by normalizing the molar flow rate of silane to that of TMGa. These ratios were 0.11, 0.22, 0.44, 0.96, and 1.92 for the five junctions, respectively. A fixed flow rate of the carbon tetrachloride was chosen to dope the $p$ sides to the same nominal level of $1.2 \times 10^{20}$ $\text{cm}^{-3}$.

The grown wafers of the tunnel junctions were first patterned on the front sides by photolithography. Ti/Pt/Au contacts were then deposited. After liftoff in acetone, the wafers were annealed on a carbon stripe at 460 °C in forming gas for 90 s. Electrical isolations were formed by directly wet etching the wafers down through the junctions in a mixture of $\text{H}_2\text{PO}_4$, $\text{H}_2\text{O}_2$, and $\text{H}_2\text{O}$ with a volume ratio of $1:1:2.5$. The annealed Ti/Pt/Au was found to be a good mask for the etching at room temperature (RT). Next, Ni/Au/Ge/Au was evaporated onto the back sides. As a final fabrication step, another annealing was performed at 430 °C for 2 min in forming gas. The ohmic contacts fabricated using such a metallization method were measured to be less than $3 \times 10^{-6}$ $\Omega \cdot \text{cm}^2$.

$I-V$ measurements were performed at RT by probing the on-wafer diodes driven by a constant voltage source. The curves given in Fig. 1 were obtained by measuring the current while varying the bias voltage. These diodes under measurement have the same area of $90 \times 200 \mu\text{m}^2$. It can be seen that the junction grown with the silane flow ratio of 0.44 is the best, having the lowest zero-bias tunnel resistance and the highest peak tunnel current. The current steps marked by the arrows will be discussed later.

The same $I-V$ measurements were carried out on a series of tunnel diodes of various sizes, which were made from the wafer of the best junction grown with a silane flow ratio

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of 0.44. A first order inverse regression was used to fit the
measured resistance that is a function of the device area,
yielding a zero-bias specific tunnel resistance of \(9.59 \times 10^{-5}\cm^{-2}\). The fitting method has been introduced in our
previously published paper.\(^1\) An average peak current den-
sity of 500 \(\text{A/cm}^2\) was obtained from the measurements as
well.

Figure 2 shows the silane doping efficiency in our
MOCVD reactor with the abovementioned growth param-
eters, which is the electron concentration of \(n\)-GaAs as a
function of the normalized silane flow ratio. The electron
concentrations were obtained at RT from Van der Pauw–Hall
measurements of single layer samples grown on semi-
insulating substrates, using the same base pressure, growth
temperature, and input V/III ratio as that for the growth of
the \(n\)-side layers of the Esaki junctions. According to this
curve, the electron concentration reaches the maximum of
\(8.76 \times 10^{18}\ \text{cm}^{-3}\) at the silane flow ratio of 0.11. Further in-
crease of the silane flow results in a decline of electron con-
centration as a result of impurity autocompensation.

The autocompensation effect is also shown in Fig. 2 by
plotting the zero-bias specific tunnel resistance for the Esaki
junctions, with the silane flow used. One can find that using
a silane flow ratio in a range from 0.44 to 0.96 can result in
low zero-bias tunnel resistances. The lowest zero-bias spe-
fic tunnel resistance we obtained was from the junction
with an \(n\)-side layer electron concentration of \(5.67 \times 10^{18}\ \text{cm}^{-3}\), grown with a silane flow ratio of 0.44. The
electron concentration of this junction is somewhat lower
than the highest concentration of \(8.76 \times 10^{18}\ \text{cm}^{-3}\) obtained
with a flow ratio of 0.11.

Consider the variation of the zero-bias specific tunnel
resistance in Fig. 2. The resistance first drops by a factor of
37.5 when the silane flow ratio increases from 0.11 to 0.44.
This could result from several effects. One is the signifi-
cantly enhanced defect-assisted tunneling,\(^1\) which is also
supported by the rapid rise of the junction excess current
(shown in Fig. 1) as the silane flow increases. Another could
be the effect of the Coulombic interactions between the
impurities.\(^1\) The attraction between \(C_{\text{As}}\) and \(S_{\text{Ga}}\) and the
repulsion between \(C_{\text{As}}\) and \(S_{\text{As}}\) are thought to form a sharper
and higher carrier concentration profile at the junction inter-
face. The third effect can be the band narrowing\(^1\) resulted
from high doping. The junction resistance remains low for
the flow ratio of 0.96. Further increase of the flow ratio re-
sulted in a significantly reduced electron concentration on
the \(n\) side, leading to a thickened tunneling barrier or the
space charge region. As a result, the zero-bias specific tunnel
resistance of the junction increased drastically.

In summary, tunneling is found to be significantly en-
hanced in Esaki junctions with \(n\)-side impurities autocom-
pressed, owing to one or all of the following effects:
impurity-assisted tunneling, Coulombic interaction, and band
narrowing. The silane flow ratio for doping the \(n\) sides was
optimized for the lowest zero-bias tunnel resistance instead
of highest electron concentration. The optimal flow ratio was
found to be far above the one required for the highest
electron concentration.

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\(^3\) K. A. Bertness, S. R. Kurtz, D. J. Friedman, A. E. Kibbler, C. Kramer, and