A Flicker-Noise-Free DC-Offset-Free Harmonic Mixer in a CMOS Process

Zhaofeng Zhang, Jack Lau

Department of Electrical & Electronic Engineering
Hong Kong University of Science & Technology
Clear Water Bay, Kowloon, Hong Kong, China

Abstract
A harmonic mixer for direct-conversion receivers is proposed and fabricated in a CMOS process. It is immune from both the flicker noise and self-mixing induced DC offset. Using the lateral bipolar transistor and the harmonic mixing technique, it achieves +15dB gain, 17.8dB NF at 10kHz frequency, -8.2dBm IIP3, +44dBm IIP2 and more than 30dB DC offset suppression. It consumes 2.2mW power at 3V.

I. INTRODUCTION
The semiconductor industry continues to challenge analog and RFIC designers with a demand for higher performance and better compatibility with a digital world. It is desirable to use a single mainstream digital CMOS process for all IC products, especially for a system on a single chip. To achieve the highest integration, direct conversion for the analogue part is the most expedient candidate of all architectures because of its simplicity, image-rejection-free and low power operation.

However, the design of CMOS direct-conversion transceivers entails many difficulties: self-mixing induced DC-offset, flicker noise, even-order distortion, I/Q mismatch, and so on [1]. The first two are the most problematic. The DC-offset can be as large as 10mV at the mixer output while the desired signal level can be only tens of µVs. Thus, the offset voltage saturates the circuits following the mixer, thereby prohibiting the amplification of the desired signal. As for the flicker noise, it not only degrades the noise performance of mixers and phase noise of oscillators, but also adds noise directly to the base band at the output of the mixer. As most modulation schemes contain significant DC and low frequency components, base band offset cancellation is generally not a viable option, especially in the case of narrow band modulation. Therefore, the bottleneck is in the mixer and a solution on this component should be sought. A good mixer can solve almost all the problems associated with direct conversion architecture.

The dynamic matching technology proposed by E. Bautista[2] helps improve IIP2 and reduce flicker noise but does not solve the DC offset problem. Zhang[3] solves the DC offset problem, but the noise performance is still not satisfactory due to the intrinsic flicker noise associated with MOS devices.

Lateral bipolar transistors are important for a CMOS based technology because they can be easily integrated into the process to achieve a BiCMOS technology without added cost. It is a good candidate for lowering the flicker noise [4].

In this paper, a novel harmonic mixer based on lateral bipolar devices will be introduced to solve flicker noise and the DC-offset problem. Firstly a lateral bipolar transistor is characterized in section II. Using this device, a mixer based on harmonic mixing is built and measured. Finally a conclusion is drawn.

II. LATERAL BIPOLAR TRANSISTOR
There are two kinds of lateral BJT available: the pure bipolar [4] and the hybrid device [5]. For hybrid BJT, it has a very large common-emitter current gain. However, flicker noise still exists because the internal MOS device is still on. For the pure bipolar device, the MOS transistor is switched off completely so it is flicker noise free. Typically the corner frequency of flicker noise is lower than 100Hz.

In a bulk n-well CMOS process, only a lateral p-n-p (LPNP) can be constructed. The n-well serves as the base, and the minimum polysilicon gate length sets the base width. A p-diffusion emitter is surrounded by a p-diffusion lateral collector. To reduce the unavoidable parasitic vertical collector current, the transistors are laid out as multi-emitter devices [4], in which each emitter is a minimum area p-diffusion contact surrounded by a polysilicon gate as shown in Fig. 1. By doing this, the ratio of lateral collector current to vertical parasitic collector current is maximized and the lateral collector current efficiency is improved. Each device is surrounded by a p+ substrate guard ring to provide the sinking ground for the parasitic current.

![Figure 1 Layout and symbol of minimum lateral bipolar transistor cell fabricated in a bulk CMOS process.](image)

Physically the LPNP can be modelled using one lateral bipolar transistor and two vertical bipolar transistors paralleled with a PMOS transistor (Fig. 2). To have a pure...
bipolar action to eliminate the flicker noise, the gate is zero-biased with respect to the emitter to prevent M1 from turning on. Both junctions of Q3 are reverse-biased, so this device is also off. However, it is impossible to directly measure the internal currents flowing in each device [6]. Using the assumption that the base currents of the internal lateral and vertical bipolar transistors are the same, it becomes possible to derive both the lateral and vertical $\beta$ required for the model.

The $Ic-Vc$ characteristics of the lateral BJT in a common emitter configuration with an 0.35$\mu$m base width can be seen in Fig. 3. The Early voltage is around 10V. The Gummel plot showing the collector $Ic$, base $Ib$, and substrate $Isub$ currents for the same device is presented in Fig. 4. For low collector current levels, an ideal exponential current-voltage behaviour is observed (i.e., 60mV/decade). This indicates that the dependence of $Ic$ on $Vb$ is similar to that of a conventional BJT. Since the thickness of the n-well is much larger than the minimum gate length, the vertical substrate current is much smaller than the lateral collector current.

Fig. 5 shows the lateral $\beta$, vertical $\beta$ and the current efficiency $\eta$. At low current densities, lateral $\beta$ is as high as 500. High level injection leads to the $\beta$ roll off. At the mA range of the collector current, it is larger than 40 which is still large enough for the applications. Vertical $\beta$ is much flatter and smaller than lateral one due to a larger base width. When the current $Ic$ is within useful range, the lateral efficiency is larger than 0.6 representing a significant improvement over the typical lateral efficiency of 0.25 to 0.50 [4].

The ac characteristics of the Lateral BJT device are also measured and the $f_T$ of the lateral bipolar is around 4GHz at 1mA. The $f_T$ can be largely improved with a silicided process and a smaller minimum gate length.

### III. HARMONIC MIXER

The conventional CMOS gilbert mixer has a large gain and a good linearity but has a bad flicker noise performance and inherent self-mixing problem. A CMOS harmonic mixer has been proposed by Zhang [3] to solve the self-mixing induced DC offset problem. It utilizes the LO’s harmonics to mix down the RF signal. Any LO leakage to the RF port will be mixed by the second harmonic of the LO to the same LO frequency and it will be filtered out at a later stage. Theoretically no DC offset will be created. However, its noise performance is still largely degraded by the severe flicker noise. To eliminate the effect of flicker noise, lateral bipolar devices
were used to replace MOS transistors at the RF stage of the mixer as shown in Fig. 6. The LO stage (m1, m2) has no flicker noise contribution at the mixer output due to the noise upconversion and common-mode operation while RF stage (q1, q2) has a very low flicker noise corner due to the bipolar mode. Consequently, the new harmonic mixer is flicker-noise-free and DC-offset-free. The current source was introduced to further improve the noise performance.

To measure the performance, the mixer is followed by an on-chip PMOS buffer which has a smaller flicker noise effect than the NMOS one. The same buffer was fabricated separately on the same die and measured for calibration and deembedding. It has 7.8 dB gain and +6dBm IIP3. The mixer performance next reported on excludes the buffer except the noise figure.

The RF signal gain is depicted in Fig. 7. Given the same bias current, a bipolar device gives a larger transconductance than an MOS transistor. Therefore, the mixer achieves a larger signal gain than do conventional MOS mixers. As the LO power increases, the gain increases dramatically due to increased time-varying transconductance. An increased injected current leads to the gain decreasing due to larger transconductance clipping when a smaller LO power is applied. However, when the LO power is large enough, the injected current helps increase the gain.

Conventional mixers have no DC-offset suppression ability because the LO leakage and RF signal lie in the same frequency band and their conversion gains are the same. But, for the harmonic mixer presented in this paper, they belong to different frequency bands and have different conversion paths and different gains. For the RF signal, the signal is mixed by the second harmonic of the LO. For the LO leakage, it is mixed by the LO itself. If the transistors at the LO stage are exactly the same and if the inputs are exactly differential, there will be no LO frequency component created in the time-varying transconductances and the gain of LO leakage will be zero. But the device mismatch is unavoidable. It can be seen from Fig. 8 that more than 30dB DC-offset suppression is achieved. The output spectrum was measured at the buffer output.

The noise performance is shown in Fig. 9. The minimum noise figure at 10kHz is below 18dB while a gilbert mixer gives around 30dB NF at this frequency. The larger the LO power, the larger the transconductance, and the better the noise performance. Current injection also improves the noise at a large LO power since the RF gain increases while the DC component of time-varying transconductance decreases.

Fig. 10 shows the linearity performance. The larger the LO power, the worse the linearity. There is a trade-off
between the linearity and the signal gain or the noise performance.

The Input-referred IP2 is very important for direct conversion applications. Two high-frequency interferers can generate a low frequency beat in the interested band in the presence of even-order distortion. Any asymmetry in the RF stage of the mixer may lead to the degradation of the IP2 performance. In order to compensate for the device mismatch in the RF stage, different DC biases were applied to the differential RF port separately. As seen from Fig. 11, if this is not done, only +18dBm IIP2 is obtained. After mismatch compensation, more than +40dBm IIP2 is achieved. The bias voltage difference is within several mVs. The spectrum was also measured at the buffer output.

The overall mixer performance is summarized in Table 1. At a +3V power supply, the mixer achieves 15dB gain and only consumes 2.2mW. The input RF bandwidth is larger than 300MHz. It can be further improved by reducing the size of the lateral bipolar devices.

Table 1: Mixer Performance Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>TSMC 3M2P CMOS0.35µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>3V</td>
</tr>
<tr>
<td>Signal gain</td>
<td>+15dB</td>
</tr>
<tr>
<td>DC offset suppression</td>
<td>&gt; 30 dB</td>
</tr>
<tr>
<td>Noise figure @ 10kHz</td>
<td>&lt; 18dB</td>
</tr>
<tr>
<td>1dB compression point</td>
<td>&gt; -20dBm</td>
</tr>
<tr>
<td>Input referred IP3</td>
<td>&gt; -9dBm</td>
</tr>
<tr>
<td>Input-referred IP2</td>
<td>&gt; +40dBm</td>
</tr>
<tr>
<td>Power consumption</td>
<td>&lt;2.2mW</td>
</tr>
</tbody>
</table>

IV. CONCLUSION

A high-gain low-power harmonic mixer in a CMOS process was fabricated using lateral bipolar and harmonic mixing techniques. Both the flicker noise and self-mixing induced DC offset were circumvented successfully. It is suitable for low power and low cost direct-conversion receivers.

REFERENCES