A CMOS SELF-MIXING-FREE FRONT-END FOR DIRECT CONVERSION APPLICATIONS

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ABSTRACT

A CMOS self-mixing-free RF front-end for direct-conversion receivers is presented, which includes a differential LNA, a ring oscillator, and I/Q double-balanced harmonic mixers and buffers. It operates at 930MHz, achieves 51dB gain and 5.8dB spot noise figure at 100kHz frequency, and consumes 53mW power. A 54dB self-mixing improvement over traditional architecture is obtained. The front-end is entirely self-mixing-free and suitable for direct-conversion applications.

I. INTRODUCTION

The growing demand for wireless products in recent years has resulted in intensive efforts to develop single chip transceivers to reduce cost, power dissipation and chip size. Of all the possible architectures, direct conversion is the most promising one for low complexity, low power and low cost single chip integration [1, 2]. However, it is plagued by the problem of large, time-varying offsets that are induced by self-mixing in the mixer. Self-mixing arises from insufficient on-chip isolation between the LO port of the mixer and the RF input port of LNA and the mixer. In addition to the static DC offset introduced, a time-varying or dynamic offset is also created when a time-varying strong interferer leaks to the LO port of the mixer or the LO leakage radiates and reflects off the moving objects back to the antenna. This changing offset is unpredictable and very difficult to be kicked off. And the magnitude of the offset created at the mixer output can be several tens of dB larger than the desired signal level [3]. It may greatly degrade the receiver BER performance, especially for those kind of modulation schemes which contain significant energy at or near the DC component. Figure 1 shows the simulated effect of the DC offset on the BER performance of a 4-FSK receiver [4]. As the offset level gets strong enough, the demodulator is eventually out of function.

So far, there are mainly five approaches to remove the DC offset. For DC-free or broad band modulation schemes, high pass filtering or AC coupling can be used. Off-chip large capacitors should be used to avoid the energy loss at the lower frequency band. However, they result in a failure to track the large time-varying offset. The second technique is to exploit the idle time intervals in digital wireless standards to carry out offset cancellation. It only works if the offset is constant during the reception of at least two bursts. Strong interferer during the interval may lead to incorrect offset measurement. For digital cancellation scheme, the offset is detected and removed digitally by time-averaging at the baseband output. It requires the baseband circuit to have enough spurious-free dynamic range to tolerate the offset. Moreover, it is also unable to cancel the dynamic offset. Recently people utilize a double-operating-frequency VCO, a localized divider and an LO buffer to reduce the leakage to the antenna and LNA, and to subsequently reduce the DC offset [5]. However, the self-mixing problem still exists due to severe substrate coupling. Holenstein [6] proposed an adaptive dual-loop algorithm to cancel the time-varying offset. The disadvantage is the introduced complexity and it is only suitable for the case that the varying offset is much larger than the signal level. It has been seen from the figure that even the offset comparable to the signal level still has a large effect on the BER performance.

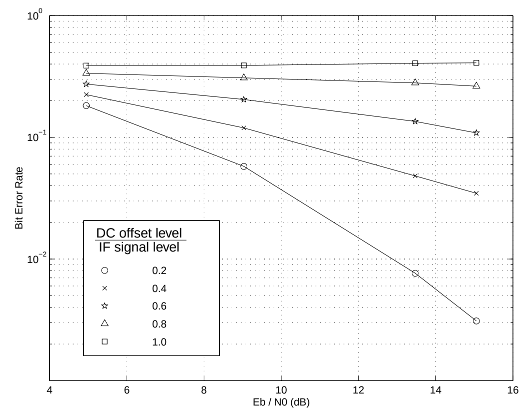

Figure 1 Effect of DC offset on the BER performance

The self-mixing originates from the mixer. In order to solve the problem more efficiently, a solution from the offset source must be found. In this paper, harmonic mixers [7] are used instead of traditional gilbert mixers in the RF front-end. Self-mixing problem is completely removed from its origin. Based on harmonic mixing, a self-mixing-free front-end suitable for direct-conversion is fabricated and measured.

II. CIRCUIT DESIGN

The block diagram of RF front-end for direct-conversion receivers is shown in Figure 2. Differential structures are used throughout the design to suppress common-mode substrate noise and interference. The image-rejection band-pass filter between LNA and the mixers is not needed any longer for direct-conversion receivers. Unlike traditional architectures, the two LO signals driving the harmonic mixer pair have 45° phase difference rather than the quadrature phase used in standard structures. Output signals can be processed by different kind of demodulators according to modulation schemes.

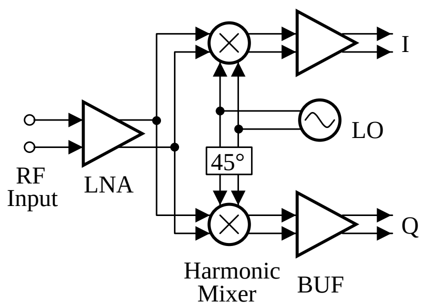

Figure 2 Direct-conversion front-end block diagram

At the RF frequency range, the non-quasi-static (NQS) phenomenon of the MOS transistor becomes important. The input impedance of the transistor has a significant but not-well-modelled real part, making it difficult to completely perform on-chip matching. In addition, the on-chip inductor consumes a large area and is sensitive to noise coupling. In our design, the matching network is done off-chip with one single inductor and a balun to convert the single-ended signal to differential. The inductive loading of LNA is realized off-chip also to boost the gain and provide better band pass filtering. The cascoded differential LNA as shown in Figure 3 provides more than 20dB gain. This large gain gives room to reduce the effect of flicker noise in the following stages although it does somewhat degrade the linearity of the receiver. The variable resistor is used to provide the mixers with a proper bias point. The transistor size is optimized both for input matching and noise performance.

The self-mixing induced DC offset is more problematic than the static DC offset caused by device mismatch. It changes with operating conditions and incoming signals. Unlike conventional mixers, a harmonic mixer [7] utilizes LO harmonics to mix down the RF signal and is theoretically free of self-mixing. The mixing principle is shown in Figure 4. Notice that there should be no coupling between the second harmonic of LO and the RF input. It can be seen from Figure 5 that the LO stage (m1-m4) acts as a frequency doubler to

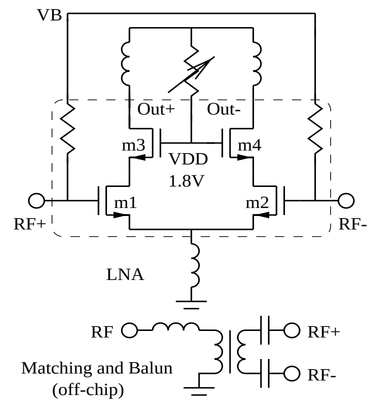

Figure 3 LNA and matching network

convert the input differential LO voltage to the current form which contains the even harmonics of LO and controls the transconductance of the RF stage. Any LO leakage to the RF port will be mixed to LO frequency again and will be filtered out at a later stage. To connect the mixer to LNA, a double balanced structure is used to improve the linearity and to provide a constant impedance to LNA. An injected current, *Ii*, helps reduce the flicker noise and improves the RF gain without introducing any noise because the transconductances of the RF stage change simultaneously and the noise due to current source and the LO stage is a common-mode signal seen at the mixer differential output. The measured harmonic mixer is self-mixing free and achieves around a 12 dB gain. To provide enough gain to reduce the noise contribution from the baseband, a buffer with 16.5dB gain is inserted after the harmonic mixer.

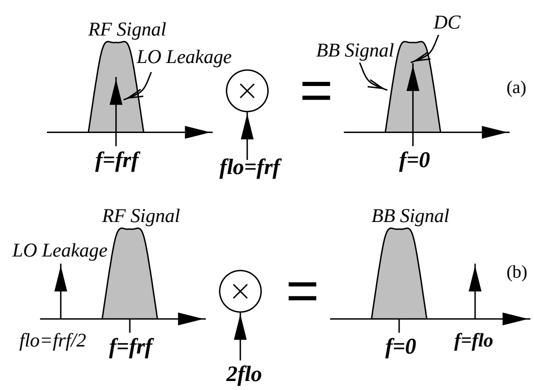

Figure 4 Mixing principle of (a) Conventional mixer (b) Harmonic mixer

Another advantage of the harmonic mixer is that it only needs a small LO swing of less than 200mV. Therefore, a 4-stage differential ring oscillator shown in Figure 6 is implemented by the source coupled logic circuit which minimizes substrate coupling. Each output is followed by an amplifier similar to the delay cell circuit to isolate the oscillator and the mixer and a source follower to give the correct mixer input bias. Eight

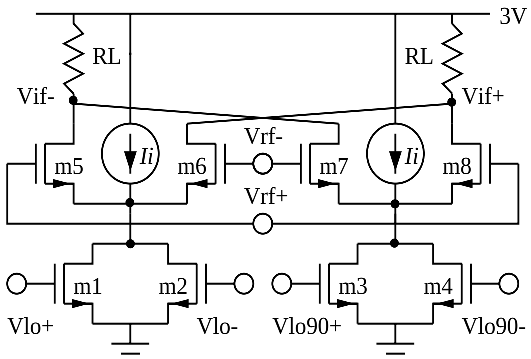

Figure 5 Double balanced harmonic mixer (f_{LO}=465MHz)

differential outputs provide the I/Q harmonic mixers with accurate 0°, 45°, 90°, 135° phase shifted LO differential input. The phase error is less than 2°.

Since the front-end is for direct conversion receivers, the flicker noise reduction is our biggest concern. Both LNA and the mixers are optimized for noise improvement while the linearity is degraded due to large LNA gain and poor mixer linearity performance. Therefore it restricts this front-end on those applications that the linearity requirement of the receiver is much relaxed.

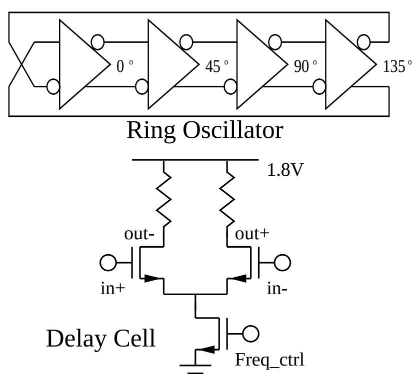

Figure 6 Differential 4-stage ring oscillator

III. MEASUREMENTS

The measured device characteristics of LNA are shown in Figure 7. The optimal FMIN and optimal associated gain *Ga* have different bias points. To minimize the noise figure, an optimal noise bias point is chosen with a small compromise on the gain. Good input matching is achieved as depicted in Figure 8 and reflection coefficient S_{11} is less than -20dB at 930MHz. It can be seen from Figure 9 that the quality factor of off-chip bond wire inductor is larger than 30 which results in a large gain and good noise performance of the front-end.

The tuning curve of the ring oscillator is shown in Figure 10. The oscillating frequency is proportional to the bias voltage

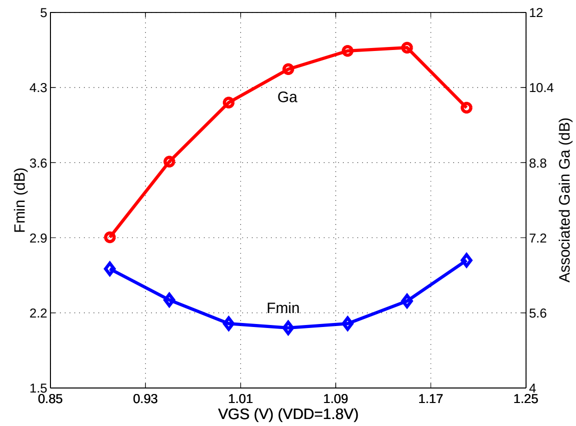

Figure 7 Device characteristics of LNA @ 930MHz.

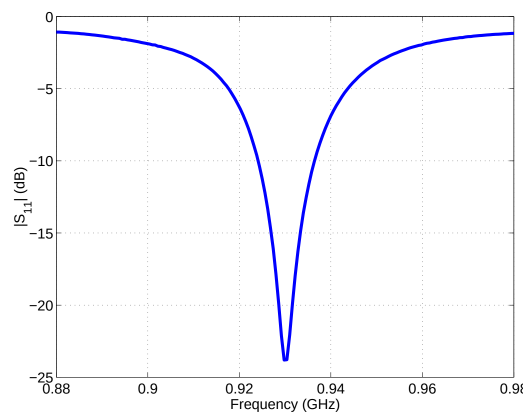

Figure 8 Input matching of the front-end

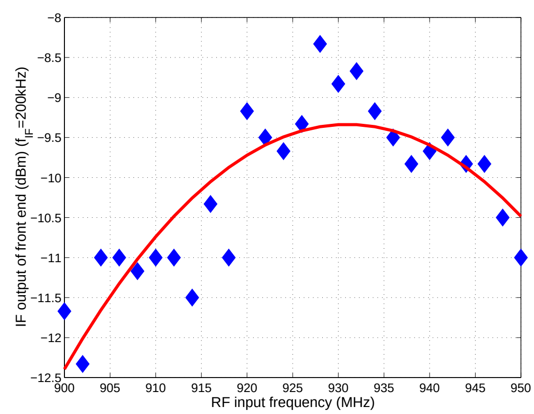

Figure 9 Resonant frequency of LC tank

and it is half of the carrier frequency.

Figure 11 gives the noise performance of the chip. The front-end with off-chip inductive loads achieves a 5.8dB noise figure including the balun loss at 100kHz. The high gain of LNA helps suppress the flicker noise. At higher frequency band, the flicker noise becomes smaller and the thermal noise dominates. The result indicates that the noise in the mixer is

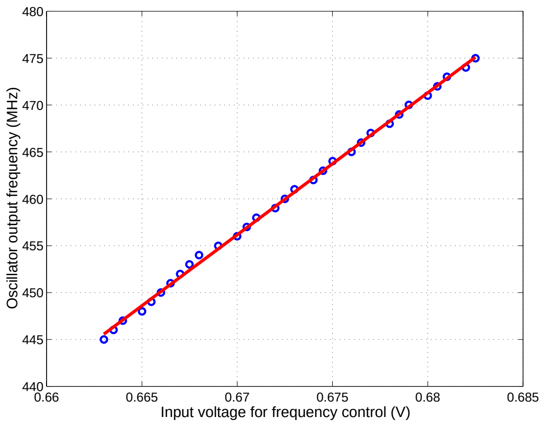

Figure 10 Measured tuning curve of ring oscillator

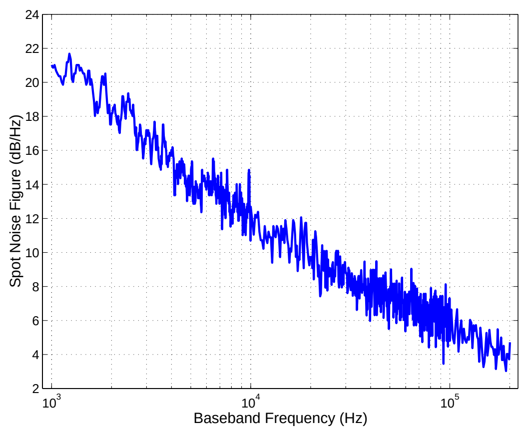

Figure 11 Noise performance of the front-end

the dominant part of the total noise spectrum.

The characteristics of CMOS direct conversion RF front-end are summarized in Table 1. It operates at 930MHz and achieves a 51dB gain, 5.8dB spot noise figure at 100kHz frequency and consumes 53mW power. The LO leakage gain is 54dB less than the RF signal gain and therefore the front-end is self-mixing free. The input-referred IP2 performance is not good enough for direct-conversion applications. It can be further improved using some kind of IM2 compensation circuitry as did in [8]. The die photo is shown in Figure 12.

IV. SUMMARY

The conventional self-mixing problem encountered in direct-conversion receivers is tackled in this paper. A CMOS self-mixing-free direct-conversion RF front-end is demonstrated.

V. REFERENCES

[1] T. Cho, et al., “A Single-Chip CMOS Direct-Conversion Transceiver for 900MHz Spread-Spectrum Digital Cordless Phones,” *ISSCC Digest of Technical Papers*, Feb. 1999.

RF/BB gain:	51.13dB
NF@100kHz:	5.8dB
IIP3:	-26dBm
IIP2:	-10dBm
Operating frequency:	930.1MHz
LO frequency:	465MHz
IQ gain mismatch:	< 0.3dB
IQ phase mismatch:	< 5°
RF/BB over LO/BB:	>54dB
Input matching:	<-20dB
Power dissipation:	52.76mW
Technology:	TSMC0.35µm 2P4M CMOS
Die area:	$0.78mm^2$

Table 1 Front-end performance summary

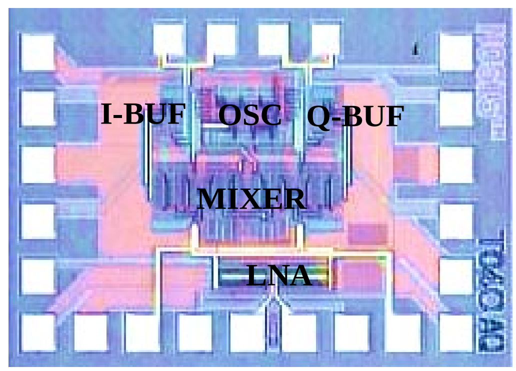

Figure 12 Die photo of the front-end

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