Performance of Poly-Si Thin Film Transistors with Ultra-Thin Ni-MILC Channel Layers

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Abstract

High-performance low temperature thin film transistors (TFTs) with ultra-thin (30nm) metal induced laterally crystallized (MILC) channel layers were characterized. Compared with the MILC TFTs with thicker (100nm) channel layers, the ones with the thinner channel layers exhibit lower threshold voltage, steeper sub-threshold slope and higher trans-conductance. Furthermore, the comparatively lower off-state leakage current and the higher on-state current of the “thin” devices also imply a higher on/off ratio. At a drain voltage of 5V, an on/off ratio of about $3 \times 10^7$ was obtained for the 30nm-TFTs, which is about 100 times better than that of the 100nm-TFTs. No deliberate hydrogenation was performed on these devices.

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Introduction

Silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect transistors with ultra-thin channel layers have various advantages. These include high mobility [1], kink elimination [2], saturation current enhancement [3], steeper sub-threshold slope and lower threshold voltage [4]. Similar beneficial effects have also been observed [5] in polycrystalline silicon (poly-Si) TFTs with ultra-thin channel layers. Little et al. [6] successfully fabricated low temperature poly-Si TFTs with 25nm thick channel by solid phase crystallization (SPC). However, the field effect mobility of the device is less than 25cm$^2$/Vs, mainly due to a significant reduction of the lateral grain size with the film thickness. Employing suitably optimized Excimer laser crystallization (ELC), Kuriyama et al. [7] showed that larger lateral grain size in ultra-thin silicon film could be realized. This makes it possible to fabricate better performing poly-Si TFTs with 50nm thick channel layers, achieving a field effect mobility as high as 280cm$^2$/Vs and an on/off ratio above $10^6$.

Unlike in SPC, where the lateral grain size is correlated to the thickness of the amorphous silicon (a-Si) layer, MILC [8] provides, without the complexity of ELC, the possibility of forming poly-Si film with large lateral grain sizes relatively independent of the film thickness. In this work, MILC-TFTs with 30nm thick channel layers were fabricated and their performance was compared to that of similar TFTs with 100nm thick channel layers.

Experimental

A schematic structure of a TFT with ultra-thin 30nm channel layer realized using a 5-mask process is shown in Figure 1. Compared with the conventional 4-mask process, the fifth mask was inserted to pattern the additional source/drain “pads” for reduced source/drain parasitic resistance.

The starting substrates were 100mm diameter, (100)-oriented silicon wafers. Following the growth of 500nm of thermal oxide, 100nm of amorphous Si (a-Si) was deposited at 550°C in a low-pressure chemical vapor deposition (LPCVD) system using SiH$_4$ as the source gas, and subsequently patterned to form the source and drain “pad” regions. A second 30nm layer of a-Si was deposited and patterned to form the channel layers. The gate insulator, consisting of 100nm of LPCVD low temperature oxide (LTO), was deposited at 425°C. This was
immediately followed by the deposition and patterning of 300nm of a-Si as the gate electrode. Phosphorus ions at a dose of $4 \times 10^{15}/\text{cm}^2$ were implanted to dope the gate and to form the self-aligned source and drain regions. After the implantation, any LTO not covered by the gate electrode was removed in buffered HF solution and 5nm of Ni was blanket deposited in an high vacuum electron-beam evaporator. Since the MILC rate was around 1.6µm/hr, the wafers were heat-treated at 500°C in an N₂ ambient for two hours to crystallize the 5µm long channels. All unreacted Ni was subsequently removed in a 40% HCl solution at 60°C. Contact holes were opened in buffered HF solution after the deposition of 500nm of LTO as the pre-metal insulation layer. The devices were sintered for 30 minutes in Forming gas at 450°C after 1µm of Al-1%Si was sputtered deposited as the metallization layer.

For comparison, normal 4-mask self-aligned MILC-TFTs with 100nm thick channel layers were fabricated. Except for the absence of the source/drain “pads”, all other process conditions were the same as those for the TFTs with the 30nm thick channel layers.

Except for the sintering in Forming gas, no other hydrogenation process was performed. This allowed the “intrinsic” behavior of the devices to be compared and studied. Electrical characterization was performed at room temperature using an HP4156 Precision Semiconductor Parameter Analyzer.

**Results and discussion**

Typical $I_d$-$V_g$ curves of the N-type TFTs with 30nm and 100nm thick channel layers are shown in Figure 2a. The channel width (W) the length (L) of the TFTs are 10µm and 5µm, respectively. Compared to those of the 100nm devices, lower minimum leakage current in the “off” state and higher drive current in the “on” state were measured on the 30nm devices - thus resulting in more than 2 orders of magnitude increase in the corresponding on/off current ratio. While it is true that the lower leakage current resulted in part from the smaller junction area in the 30nm devices, this alone cannot account for a reduction that is significantly more than 3 times. It is also a consequence of the better gate control of the potential through the reduced thickness of the 30nm channel layer. This improved control is also responsible for the correspondingly higher drive current.
The linear trans-conductance (g_m) of the two kinds of devices are extracted and plotted in Figure 2b. Clearly, the 30nm device exhibits a larger peak g_m than the 100nm device. The field-effect mobility, \( \mu_{FE} \), of the devices can be calculated by assuming the validity of the following equation for the MILC-TFTs:

\[
g_m = \mu_{FE} C_{ox} \frac{W}{L} V_{ds},
\]

where \( C_{ox} \) is the gate capacitance per unit area. A maximum \( \mu_{FE} \) of 110cm^2/Vs is estimated for the 30nm device, which is about 40% higher than the 80cm^2/Vs estimated for the 100nm device. This improvement in \( \mu_{FE} \) could be attributed to the reduced vertical field in the ultra-thin channel layers [1].

Typical I_d-V_ds curves of the TFTs with 30nm and the 100nm thick channel layers are shown in Figures 3a and 3b, respectively. At any given \( V_g \), the 30nm devices exhibit higher on-current because of their higher mobility and lower threshold voltage. The absence of current pinching in the 30nm devices indicates that the parasitic source/drain resistance does not limit the saturation I_d to any significant extent. Interestingly, while the family of I_d curves for the 100nm device shows almost ideal I_d saturation behavior, that of the 30nm device shows a tendency of a soft breakdown at \( V_{ds} = 14V \). Similar phenomena have been observed in SOI devices [9], in which higher drain field occurs in devices with thinner channel layers.

In Table 1, the performance of the TFTs fabricated in this work and that of the non-optimized and optimized MILC-TFTs reported in Ref. [10] are compared. The threshold voltage is defined as the gate voltage required to achieve a normalized drain current of \( I_d = (W/L)x10^{-7}A \) at \( V_{ds} = 0.1V \). The on/off ratio is obtained from the I_d-V_g at \( V_{ds} = 5V \) and defined as the ratio of the I_{ds} at \( V_g =20V \) to the minimum I_{ds}.

The leakage current in the MILC TFTs was believed to result from the higher Ni concentration near the drain junction [10]. By using an off-set structure to separate regions of Ni concentration from the metallurgical junction, Ihn et al. [10] achieved significant reduction in the off-current. The low off-current measured on the 30nm devices indicates that the use of thin channel layers could provide an alternative approach to off-current reduction. If the off-set structure were combined with the thin channel layers, further decrease in the off-current and a corresponding increase in the on/off ratio would be expected.
**Summary**

High performance TFTs with 30nm and 100nm thick channel layers have been successfully fabricated using nickel induced crystallization of a-Si. The highest temperature used was 550°C for the a-Si deposition. If alternative low temperature techniques of a-Si formation were employed, such as replacing SiH$_4$ with Si$_2$H$_6$ [10] or using plasma activation, this would have been a 500°C process – limited only by the MILC temperature.

Compared with the TFTs with 100nm thick channel layers, the TFTs with 30nm channel layers show an improvement of over 40% in the field effect mobility. The devices exhibit not only lower off-current but also the higher on-current, resulting in an increase of 100 times in the on/off ratio. The threshold and the sub-threshold slope are also significantly improved. The possible reasons of the improvements have been discussed.

**Acknowledgments**

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References


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Figure 3. \( I_d-V_d \) curves of the a) 30nm and b) 100nm thick channel layer TFTs.
Table 1.

<table>
<thead>
<tr>
<th></th>
<th>Devices in this work W/L=10/5 (µm)</th>
<th>Devices reported in Ref. [10] W/L=10/10 (µm)</th>
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<tr>
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<td>100nm thick channel layer</td>
<td>30nm thick channel layer</td>
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<td>$\mu_F$ (cm$^2$/Vs)</td>
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<td>$V_T$ (V)</td>
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<td>$S$ (V/decade)</td>
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<td>$I_{off}$ (pA/µm)</td>
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<td>On/off ratio</td>
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</tr>
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</tr>
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<td>$V_T$ (V)</td>
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<td>$S$ (V/decade)</td>
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<td>$I_{off}$ (pA/µm)</td>
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<td>On/off ratio</td>
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<td>$V_T$ (V)</td>
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<tr>
<td>On/off ratio</td>
<td>1.2 x 10$^6*$</td>
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</table>

- Estimated from the reported $I_d$-$V_g$ curves.
Figure 1.

Drain  Gate  Source

100nm Thick Pad  100nm LTO

30nm MILC Channel Layer
Figure 2a.

Drain Current (A) vs. Gate Voltage (V) for different values of $V_{ds}$: $V_{ds} = 0.1V$ and $V_{ds} = 5V$.

- 30nm Channel Layer
- 100nm Channel Layer

$W/L=10/5$ (µm)
Figure 2b.

Gate Voltage (V) vs. Trans-Conductance (µS) for channel layers of different thicknesses at $V_{ds} = 0.1V$.
Figure 3a.

 Drain Current (mA) vs. $V_{ds}$ (V)

W/L=10/5 ($\mu$m)
30nm Thick Channel Layer

$V_g = 20V$
15V
10V
5V

$V_{ds}$ (V)
Figure 3b.

![Graph showing Drain Current (mA) vs. Vds (V) for different Vg values.]

- **W/L=10/5 (µm)**
- **100nm Thick Channel Layer**

- **Vg=20V**
- **15V**
- **10V**

*Axes:*
- Y-axis: Drain Current (mA)
- X-axis: Vds (V)