Channel Engineering of III-Nitride HEMTs for Enhanced Device Performance

by

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# TABLE OF CONTENTS

Title Page ................................................................. i
Authorization Page ....................................................... ii
Signature Page ........................................................... iii
Acknowledgements ....................................................... iv
Table of Contents ........................................................ vi
List of Figures ........................................................... ix
List of Tables ............................................................ xvi
Abstract ................................................................. 1

Chapter 1  Introduction .................................................. 4
  1.1 Basic Principles of HEMTs ........................................ 4
  1.2 AlGaN/GaN-based HEMTs ........................................ 14
  1.3 Limitations in the Conventional AlGaN/GaN HEMTs ............ 20
     1.3.1 Linearity Limitation ....................................... 20
     1.3.2 Limitation of Carrier Confinement ....................... 22
  1.4 Objective of This Work ......................................... 23

Chapter 2  $\text{Al}_{x}\text{Ga}_{1-x}\text{N/Al}_y\text{Ga}_{1-y}\text{N/GaN}$ Composite-Channel HEMTs (CC-HEMTs) with Enhanced Linearity .................................................. 25
  2.1 Channel Engineering for Enhanced Linearity in GaN-based HEMTs ........ 25
  2.2 Design of the $\text{Al}_{x}\text{Ga}_{1-x}\text{N/Al}_y\text{Ga}_{1-y}\text{N/GaN}$ CC-HEMTs ............... 28
  2.3 Material Growth and Device Fabrication ....................... 34
2.3.1 Al_{0.3}Ga_{0.7}N/Al_{0.05}Ga_{0.95}N/GaN CC-HEMTs Growth ........................................... 34

2.3.2 Al_{x}Ga_{1-x}N/Al_{y}Ga_{1-y}N/GaN CC-HEMT Device Fabrication ....................... 38

2.4 Device Characteristics .................................................................................. 41

2.4.1 DC Characteristics .................................................................................. 41

2.4.2 RF Small-Signal Characteristics ............................................................. 46

2.4.3 Power Performance and Linearity Characteristics ................................. 51

2.5 Summary .................................................................................................... 57

Chapter 3 AlGaN/GaN/InGaN/GaN Double Hetero-Junction HEMTs (DH-HEMTs) with
Improved Carrier Confinement ..................................................................... 58

3.1 Channel Engineering for Improved Carrier Confinement in GaN-based HEMTs
...................................................................................................................... 58

3.2 Design of the Al_{x}Ga_{1-x}N/GaN/In_{y}Ga_{1-y}N/GaN DH-HEMTs ............... 63

3.3 Material Growth and Device Fabrication .................................................. 67

3.3.1 Al_{0.3}Ga_{0.7}N/GaN/In_{y}Ga_{1-y}N/GaN DH-HEMTs Growth ..................... 67

3.3.2 Al_{x}Ga_{1-x}N/GaN/In_{y}Ga_{1-y}N/GaN DH-HEMT Device Fabrication ....... 71

3.4 Device Characteristics .................................................................................. 71

3.4.1 DC Characteristics .................................................................................. 71

3.4.2 Small-signal RF Characteristics ............................................................. 74

3.4.3 Large signal RF Characteristics: Power and Linearity ......................... 78

3.5 Summary .................................................................................................... 79

Chapter 4 Enhancemnt-mode HEMTs on AlGaN/GaN/InGaN/GaN DH-HEMTs with
State-of-the-Art Performances ..................................................................... 81
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1</td>
<td>Motivation for the AlGaN/GaN-based Enhancement-mode Devices</td>
<td>81</td>
</tr>
<tr>
<td>4.2</td>
<td>E-mode AlGaN/GaN HEMTs Fabrication</td>
<td>82</td>
</tr>
<tr>
<td>4.3</td>
<td>Material Preparation and Device Fabrication</td>
<td>86</td>
</tr>
<tr>
<td>4.4</td>
<td>Device Characteristics</td>
<td>87</td>
</tr>
<tr>
<td>4.4.1</td>
<td>DC Characteristics</td>
<td>87</td>
</tr>
<tr>
<td>4.4.2</td>
<td>RF Small-signal and Large-signal Characteristics</td>
<td>89</td>
</tr>
<tr>
<td>4.4.3</td>
<td>Noise Characteristics</td>
<td>92</td>
</tr>
<tr>
<td>4.5</td>
<td>Summary</td>
<td>95</td>
</tr>
<tr>
<td>Chapter 5</td>
<td>Conclusions</td>
<td>96</td>
</tr>
<tr>
<td>5.1</td>
<td>Conclusion</td>
<td>96</td>
</tr>
<tr>
<td>5.2</td>
<td>Suggestions for Future Work</td>
<td>99</td>
</tr>
<tr>
<td></td>
<td>References</td>
<td>101</td>
</tr>
<tr>
<td>Appendix A</td>
<td>Process Flow for the Fabrications of GaN HEMTs</td>
<td>111</td>
</tr>
<tr>
<td>Appendix B</td>
<td>Device Characterization</td>
<td>116</td>
</tr>
<tr>
<td>Appendix C</td>
<td>The Extraction of Small-Signal Equivalent Circuit</td>
<td>127</td>
</tr>
<tr>
<td>Appendix D</td>
<td>Publication List</td>
<td>136</td>
</tr>
</tbody>
</table>
LIST OF FIGURES

Fig. 1.1.1 Schematic of an AlGaAs/GaAs HEMT and the corresponding energy-band profile. ................................................................. 5

Fig. 1.1.2 Energy-band diagram of the metal/n-AlGaAs/GaAs system and the electrostatic field distribution in the AlGaAs layer at the threshold voltage and $V_{G_{\text{max}}}$ . ........................................................................................................ 6

Fig. 1.1.3 Gate-bias-modulated conduction band diagram and 2DEG concentration of an AlGaAs/GaAs HEMT. ............................................. 7

Fig. 1.1.4 Typical DC I-V characteristics of an AlGaAs/GaAs HEMT: (a) output curve; (b) transfer curve. ......................................................... 8

Fig. 1.1.5 Equivalent circuit model for a HEMT, the intrinsic circuit model is enclosed by the dashed line. ......................................................... 9

Fig. 1.1.6 The physical origin of the elements in the equivalent circuit model of HEMT. ............................................................................... 10

Fig. 1.1.7 Schematic representation of a HEMT operating in Class A. ............ 13

Fig. 1.2.1 Bandgap of hexagonal ($\alpha$-phase) InN, GaN and AlN versus lattice constant $a_0$. .............................................................................. 14

Fig. 1.2.2 Crystal structure of the Ga-face (left) and N-face (right) wurtzite GaN. ......................................................................................... 16

Fig. 1.2.3 Band profiles of the AlGaN/GaN heterostructures with different AlGaN thicknesses, which demonstrates the surface states’ contribution to the 2DEG formation. ......................................................... 17

Fig. 1.2.4 Historical progress in GaN transistor technology: (a) Power density of AlGaN/GaN HEMTs versus year; (b) Total Power of AlGaN/GaN HEMTs versus year. .............................................................. 19

Fig. 1.3.1 (a) Typical transfer and transconductance characteristics of a conventional AlGaN/GaN HEMT; (b) Distortion in the output signal due to the non-linear $G_m$ at high current levels. ......................................... 21
Fig. 1.3.2 Schematic conduction band profile of the conventional AlGaN/GaN HEMTs, with some carriers spill over to buffer. .......................................... 22

Fig. 2.1.1 Schematic conduction band profile (E_C) and the transverse electrical-field (E_T) distribution in the conventional AlGaN/GaN system............... 25

Fig. 2.1.2 Band profiles and transverse electrical filed (E_T) distribution in (a) the conventional AlGaN/GaN HEMT and (b) the desired HEMT structure which employs a different channel material. ........................................ 27

Fig. 2.1.3 Schematic band profile carrier distribution of an Al_xGa_{1-x}N/Al_yGa_{1-y}N/GaN (x > y) HEMT structure. ....................................................... 28

Fig. 2.4.1 (a) Layout and (b) microscopy photo of the small device for DC characterizations. ........................................................................ 42

Fig. 2.4.2 DC I_{DS}-V_{GS} and G_m-V_{GS} characteristics: (a) conventional HEMT; (b) structure A (CC-HEMT); (c) structure B (CC-HEMT); (d) structure C (CC-HEMT). ................................................................. 42

Fig. 2.4.3 Layout of gated-TLM pattern for the extraction of source access resistance ................................................................................ 44

Fig. 2.4.4 The separated contributions to the resistance between two TLM pads. ....................................................................................... 45

Fig. 2.4.5 Gate-bias-dependent (a) source access resistance (R_S) and (b) channel resistance (R_{CH}), extracted via gated-TLM measurements.............. 46

Fig. 2.4.6 Gate-bias-dependent source access resistance obtained in ref [41].... 46

Fig. 2.4.7 Equivalent small-signal circuit model for AlGaN/GaN HEMTs........ 47

Fig. 2.4.8 Bias-dependent G_m curve extracted from on-wafer S-parameter measurements (f = 2 GHz) for 1 μm × 100 μm CC-HEMT device (structure B). ........................................................................ 47

Fig. 2.4.9 Bias-dependent cutoff frequencies for 1 μm × 100 μm CC-HEMT device (structure B): (a) f_T and (b) f_{max}. ........................................ 48

Fig. 2.4.10 Gate-bias dependent cutoff frequencies (f_T and f_{max}) for 1 μm × 100 μm CC-HEMT (structure B) with a drain bias of 10 V. ............... 49
Fig. 2.4.11 Bias-dependent (a) $C_{gs}$ and (b) $C_{gd}$ extracted from on-wafer S-parameter measurements ($f = 2$ GHz) for $1 \mu m \times 100 \mu m$ CC-HEMT device (structure B). .............................................. 50

Fig. 2.4.12 The sum of extracted bias-dependent $C_{gs}$ and $C_{gd}$ (frequency = 2 GHz) for $1 \mu m \times 100 \mu m$ CC-HEMT device (structure B). .............................................. 50

Fig. 2.4.13 Extraction of the effective channel transit delay from the measured S-parameters for $1 \mu m \times 100 \mu m$ CC-HEMT device (structure B). ...... 50

Fig. 2.4.14 Power sweep measurement by a load-pull system at 2 GHz on $1 \mu m \times 100 \mu m$ devices on the three CC-HEMT structures, with a drain supply voltage of 25 V and a gate bias of -3.5 V. ......................................................... 52

Fig. 2.4.15 Pulse (circles) mode I-V characteristics of the CC-HEMT structures, with a DC bias of $V_{DS} = 25$ V and $V_{GS} = -3.5$ V. ............................................................... 53

Fig. 2.4.16 IM3 results of the CC-HEMT structures with a fundamental frequency of 2 GHz and an offset of 1 MHz: (a) 3-nm AlGaN; (b) 6-nm AlGaN; (c) 9-nm AlGaN. ................................................................. 54

Fig. 2.4.17 ACPR and AltCPR versus backoff power in conventional and CC-HEMT. ........................................................................................................ 56

Fig. 2.4.18 ACPR and AltCPR versus output power in conventional and CC-HEMT. ................................................................................................. 56

Fig. 3.1.1 Two possible band profiles for improved carrier confinement: (a) AlGaN/GaN/AlGaN/GaN double-heterostructure; and (b) AlGaN/InGaN/GaN HEMTs. ................................................................. 59

Fig. 3.1.2 Schematic band profiles of (a) AlGaN/GaN and (b) InGaN/GaN heterojunctions. ................................................................................. 61

Fig. 3.1.3 Schematic conduction band profile of an AlGaN/GaN/InGaN/GaN DH-HEMT structure. ........................................................................... 61

Fig. 3.2.1 Calculated conduction band profiles of the AlGaN/GaN/InGaN/GaN DH-HEMT structures with different GaN channel layer thicknesses. 65

Fig. 3.2.2 (a) Calculated conduction band profiles of the DH-HEMTs with different indium composition (5% and 10%) and the conventional AlGaN/GaN HEMTs; (b) a close-up of the InGaN layer. .......... 67
Fig. 3.3.1  Schematic cross-sectional diagram of the Al$_{0.3}$Ga$_{0.7}$N/GaN/In$_2$Ga$_{1-y}$N/GaN DH-HEMT device ................................................................. 68

Fig. 3.3.2  (a) SIMS analysis result of the InGaN-notch DH-HEMT (10% In) wafer grown in a MOCVD system. An obvious indium peak with a FWHM of 3.2 nm can be observed; (b) TEM picture of the InGaN-notch DH-HEMT (10% In). A well-defined interface between the GaN channel layer and the InGaN-notch layer can be found......................... 69

Fig. 3.3.3  C-V characteristics of the InGaN-notch DH-HEMTs with different indium composition, which is measured at 100 kHz through a Schottky diode fabricated on the wafer: (a) 5% indium; (b) 10% indium............. 70

Fig. 3.4.1  DC characteristics of the InGaN-notch DH-HEMTs, compared with the conventional one: (a) $I_{DS}$-$V_{GS}$ and $G_m$-$V_{GS}$ curves with a drain bias of 10 V, about one order of magnitude lower leakage current is obtained on the InGaN-notch DH-HEMTs; (b) $I_{GD}$-$V_{GD}$ curves, the InGaN-notch ones also exhibit lower gate leakage current ............................................. 73

Fig. 3.4.2  AFM pictures of the surface of (a) conventional AlGaN/GaN (b) InGaN-notch DH-HEMT (10% In).......................................................... 74

Fig. 3.4.3  RF small signal characteristics of 1 μm × 100 μm InGaN-notch H-HEMT devices with 5% and 10% indium composition: (a) frequency-dependent $|h_{21}|^2$ and MAG/MSG curves extracted from the measured S-parameters, the bias point is chosen to maximize the cutoff frequencies; (b) bias-dependent $f_T$ and $f_{max}$ curves with a $V_{DS}$ fixed at 10 V.......... 75

Fig. 3.4.4  Bias-dependent output resistance ($R_{DS}$) curves extracted from on-wafer S-parameter measurements ($f = 2$ GHz) for 1 μm × 100 μm InGaN-notch DH-HEMT and conventional HEMT devices ............................... 76

Fig. 3.4.5  Channel transient characteristics of the InGaN-Notch HEMT: (a) 5%-indium, only one delay time; (b) 10%-indium, two different delay times can be observed .............................................................. 77

Fig. 3.4.6  Power performances of the 1 μm × 100 μm DH-HEMT devices with different indium compositions: (a) 5% indium; (b) 10% indium. The gate bias is -2.5 V and the drain bias is 35 V................................. 78

Fig. 3.4.7  Three-order inter-modulation (IM3) measurement results of 1 μm × 100 μm DH-HEMT with different indium compositions: (a) 5% indium; (b) 10% indium ................................................................ 79
Fig. 4.2.1 Schematic conduction band profiles of (a) conventional D-mode AlGaN/GaN HEMTs, and (b) E-mode AlGaN/GaN HEMTs in which the 2DEG channel is depleted by fixed negative charges in the barrier.

Fig. 4.2.2 Calculated conduction band profiles with different fixed negative charge distributions, with the distribution profiles in the insets: (a) conventional D-mode HEMTs; (b) constant distribution; (c) linear distribution; and (d) Gaussian distribution.

Fig. 4.2.3 Principle of CF₄ plasma treatment on conventional AlGaN/GaN D-mode HEMTs, where the fixed F' in AlGaN barrier can deplete the 2DEG channel.

Fig. 4.4.1 DC characteristics of the D-mode and E-mode DH-HEMTs: (a) $I_{DS}$-$V_{DS}$ curves, for D-mode, $V_{GS}$ starts from +1 V with a step of -1 V, for E-mode, $V_{GS}$ starts from +2.5 V with a step of -0.5 V; (b) $I_{DS}$, $G_{m}$-$V_{GS}$ curves, the drain bias is 10 V.

Fig. 4.4.2 RF small signal characteristics of 1 µm × 100 µm D-mode and E-mode DH-HEMT devices: (a) frequency-dependent $|h_{21}|^2$ and MAG/MSG curves extracted from the measured S-parameters, the bias point is chosen to maximize the cutoff frequencies; (b) bias-dependent $f_T$ and $f_{max}$ curves with $V_{DS}$ fixed at 10 V.

Fig. 4.4.3 Power performances of 1 µm × 100 µm (a) E-mode and (b) D-mode DH-HEMT devices measured at 2 GHz with a drain supply voltage of 35 V. For E-mode one, $G_{Linear} = 26$ dB, $P_{max} = 3.12$ W/mm, PAE = 49%; for D-mode one, $G_{Linear} = 25.5$ dB, $P_{max} = 3.46$ W/mm, PAE = 44%. .. 91

Fig. 4.4.4 Two-tone measurement result of a 1 µm × 100 µm E-mode DH-HEMT device, with an OIP3 of 34.7 dBm.

Fig. 4.4.5 Bias-dependent minimum noise figure and associated gain of a 1 µm (a) D-mode (b) E-mode DH-HEMTs.

Fig. 4.4.6 (a) Gate leakage current of D-mode and E-mode DH-HEMTs; (b) Conduction band profile of E-mode DH-HEMTs.

Fig. 4.4.6 Frequency-dependent noise characteristics of the D-mode and E-mode DH-HEMTs with a gate length of 1µm: (a) $N_{Fmin}$; (b) $\Gamma$; (c) $\tau_{n}$; and (d) $G_{a}$. .. 94
Fig. B.1  (a) Configuration of the static DC measurement with a semiconductor parameter analyzer; (b) the shape of the device for the static DC measurement. ................................................................. 116

Fig. B.2  (a) Configuration of the dynamic IV measurement with a dynamic IV analyzer; (b) the shape of the device for the dynamic IV measurement; (c) the shape of the GSG probe for RF measurements. ......................... 118

Fig. B.3  (a) Configuration of the CV measurement with a LCR meter and a semiconductor parameter analyzer; (b) the shape of Schottky diode for the CV measurement.................................................. 119

Fig. B.4  Configuration of the S-parameters measurement with a vector network analyzer (VNA) and a DC bias source controlled by PC. ............... 120

Fig. B.5  SOLT calibration standards for on-wafer RF small-signal measurement. ......................................................................................... 120

Fig. B.6  The shape of the “open” pad for device de-embedding..................... 121

Fig. B.7  Configuration of the large-signal power measurement, including a load-pull system, a signal generator, a DC bias source, and a power meter controlled by a PC................................................................. 122

Fig. B.8  Configuration of the two-tone large-signal measurement, including a load-pull system, two signal generators, a DC bias source, a power meter, and a spectrum analyzer controlled by a PC............... 124

Fig. B.9  Configuration of the ACPR measurement, including a load-pull system, a signal generator which provides modulated RF signal, a DC bias source, a power meter, and a spectrum analyzer controlled by a PC. 125

Fig. B.10 The definition of the ACPR, where the signal is a standard WCDMA modulated signal............................................................... 125

Fig. B.11 Configuration of the noise characterization system, including a load-pull system, a DC bias source, a noise source, and a noise figure analyzer controlled by a PC.................................................. 126

Fig. C.1  Small-signal equivalent circuit of field effect transistor................. 127

Fig. C.2  Method for extracting the device intrinsic Y matrix....................... 129
Fig. C.3 Sketch of the distributed RC network under the gate electrode yielding equations (C.9), (C.10), and (C.11) ......................................................... 130

Fig. C.4 Evolution of the $Z_{ll}$ real part as a function of $1/I_g$ ........................................... 132

Fig. C.5 Small-signal equivalent circuit of a FET at zero drain bias voltage and gate voltage lower than the pinchoff voltage ........................................... 134
## LIST OF TABLES

<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Table 1-1</td>
<td>Advantages of the HEMT structure.</td>
<td>8</td>
</tr>
<tr>
<td>Table 1-2</td>
<td>Lattice constants, bandgaps and binding energies of hexagonal InN, GaN and AlN.</td>
<td>15</td>
</tr>
<tr>
<td>Table 1-3</td>
<td>Historical Development of GaN-based HEMTs.</td>
<td>18</td>
</tr>
<tr>
<td>Table 1-4</td>
<td>Competitive advantages of GaN devices.</td>
<td>19</td>
</tr>
<tr>
<td>Table 2-1</td>
<td>Hall measurement results of the CC-HEMT structures.</td>
<td>36</td>
</tr>
<tr>
<td>Table 2-2</td>
<td>$G_m$ characteristics of the CC-HEMT and conventional HEMT devices.</td>
<td>44</td>
</tr>
<tr>
<td>Table 2-3</td>
<td>3GPP WCDMA key specifications.</td>
<td>55</td>
</tr>
</tbody>
</table>
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for Enhanced Device Performance

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ABSTRACT

Since the first demonstration of the AlGaN/GaN high electron mobility transistor (HEMT) over a decade ago, there has been rapid development in wide bandgap GaN-based materials and devices. Owing to their unique capabilities of achieving high breakdown voltage and high current density at microwave frequencies, AlGaN/GaN HEMTs are emerging as the promising candidates for radio-frequency (RF) and microwave power amplifiers. With tremendous progresses made during the last decade in material quality and device processing, AlGaN/GaN HEMTs have been improved significantly in both DC and RF performances. Meanwhile, more advanced device structures are being explored for further performance improvement. For employing GaN-based HEMTs as the high frequency and high power microwave devices, the limitations of the conventional AlGaN/GaN HEMTs emerge quickly. Two of the most important limitations need to be overcome are the device linearity
and buffer isolation. Up to now, significant efforts have been made to optimize or modify the gate barrier layer and improve the crystal quality of the buffer layer. The optimization of another important part of the HEMT, namely the channel region, only starts to attract attention recently.

In this work, several novel GaN-based HEMT structures were proposed by explicitly focusing on the channel region. Based on extensive band profile simulation, two kinds of new HEMT structures, Al$_x$Ga$_{1-x}$N/Al$_y$Ga$_{1-y}$N/GaN composite-channel HEMTs (CC-HEMTs) and AlGaN/GaN/InGaN/GaN double-heterojunction HEMTs (DH-HEMTs), were designed and fabricated. The composite-channel HEMT shows significantly improved linearity. They exhibited a peak transconductance of 150 mS/mm, a peak current gain cutoff frequency ($f_T$) of 12 GHz and a peak power gain cutoff frequency ($f_{max}$) of 30 GHz. For devices grown on sapphire substrate, a maximum power density of 3.4 W/mm and a power-added efficiency (PAE) of 43% were obtained at 2GHz. The output third-order intercept point (OIP3) was 33.2 dBm from two-tone measurement at 2GHz. The AlGaN/GaN/InGaN/GaN DH-HEMT features an InGaN-notch embedded in the channel region. Assisted by the InGaN layer's polarization field, an additional potential barrier is introduced between the channel and buffer, leading to enhanced carrier confinement and improved buffer isolation. A peak transconductance of 230 mS/mm, a peak current gain cutoff frequency ($f_T$) of 14.5 GHz, and a peak power gain cutoff frequency ($f_{max}$) of 45.4 GHz were achieved. The off-state source-drain leakage current was as low as ~5 µA/mm at $V_{DS}$ = 10 V. For the devices on sapphire substrate, a maximum power
density of 3.4 W/mm and a PAE of 44% were obtained at 2GHz. The DH-HEMT was further implemented in enhancement-mode (E-mode) operation, required for single-polarity supply voltage RFICs and MMICs. State-of-the-art RF power performance was demonstrated in E-mode GaN-based HEMTs for the first time. Noise characteristics of E-mode GaN-based HEMTs were also explored for the first time.
CHAPTER 1
INTRODUCTION

1.1 Basic Principles of HEMTs

The high electron mobility transistor (HEMT), which is also named as heterostructure field-effect transistor (HFET), modulation doped field-effect transistor (MODFET), two-dimensional electron gas field-effect transistor (TEGFET), or selectively doped heterostructure transistor (SDHT), was invented about 20 years ago. The first HEMT device was reported in 1980 [1], after the successful growth of modulation doped AlGaAs/GaAs heterostructure [2]. By employing two different semiconductor materials with different band-gaps, an electron potential well is formed at the hetero-interface between AlGaAs and GaAs. The electrons are confined in this potential well to form a two-dimensional electron gas (2DEG). Due to the two-dimensional feature of the electrons in this conduction channel, enhanced carrier mobility can be achieved.

Earlier HEMT structures were constructed on the AlGaAs/GaAs system, which have been widely studied and used in radio frequency (RF)/microwave communication applications. The fundamental characteristic of the HEMT structure is the conduction band offset between the materials which construct the barrier and channel layers, that is, the barrier layer has a higher conduction band while the channel layer has a lower one. A potential well is then formed which can contain a
large number of electrons to form a 2DEG channel at the hetero-interface due to this conduction band offset. The schematic structure and the energy-band profile of a AlGaAs/GaAs HEMT are shown in Fig. 1.1.1 [3]. In this case, the electrons in the 2DEG channel are provided by the modulation doped barrier layer. The electrons are separated from the ionized donors by the potential barrier at the hetero-interface and confined in a two-dimensional conduction channel, which can reduce the scattering between the carriers and the ionized donors. This feature ensures a high electron density and mobility, which make HEMTs promising for high frequency and high power applications.

![Schematic structure of an AlGaAs/GaAs HEMT and the corresponding energy-band profile.](image)

Fig. 1.1.1 Schematic structure of an AlGaAs/GaAs HEMT and the corresponding energy-band profile.

In a HEMT, by placing a Schottky barrier (metal/semiconductor) gate above the doped AlGaAs barrier layer, the 2DEG sheet charge concentration can be controlled by applying an appropriate bias voltage. Fig. 1.1.2 shows the energy-band diagram of the metal/AlGaAs/GaAs system and the electrostatic field distribution in the AlGaAs barrier layer at threshold voltage and maximum gate bias [4]. Where \( n_{so} \) is the
maximum 2DEG sheet carrier concentration, \( d \) is the thickness of the n-doped AlGaAs barrier, \( d_i \) is the thickness of the undoped AlGaAs spacer, \( \Delta d \) is the mean distance of the 2DEG from the AlGaAs/GaAs hetero-interface. When the gate bias exceeds the maximum value, \( V_{G,\text{max}} \), a zero-field or conduction region is created near the center of the AlGaAs layer. With increasing the forward gate bias, this region forms a parasitic MESFET and effectively shields the 2DEG channel of the HEMT. Then the useful gate bias swing (\( \Delta V_G \)) without pushing the AlGaAs layer into conduction is [5]:

\[
\Delta V_G = (V_{G,\text{max}} - V_{\text{TH}})
\]

\[
= \frac{q n_s \alpha}{\varepsilon} (d + d_i + \Delta d)
\]

Fig. 1.1.2 Energy-band diagram of the metal/n-AlGaAs/GaAs system and the electrostatic field distribution in the AlGaAs layer at the threshold voltage and \( V_{G,\text{max}} \).
Fig. 1.1.3 demonstrates the mechanism of the gate-controlled 2DEG channel in an AlGaAs/GaAs HEMT [3]. With a zero gate bias, there is a 2DEG accumulated at the hetero-interface, that is, the channel is on. By increasing the gate bias, the conduction band is modulated and more electrons accumulated in the 2DEG channel, which provides higher sheet carrier density and larger current density in the channel. When the gate bias is lowered below the threshold voltage ($V_{TH}$), the channel is depleted and there are no electrons in the channel, that is, the channel is pinched off and no current can go through from the drain to the gate.

Fig. 1.1.3 Gate-bias-modulated conduction band diagram and 2DEG concentration of an AlGaAs/GaAs HEMT.
With a Schottky contact serves as the gate electrode and two ohmic contacts as the source and drain electrodes, a field effect transistor (FET) can be formed on an AlGaAs/GaAs wafer. The DC output and transfer current-voltage (I-V) characteristics of a typical AlGaAs/GaAs HEMT device are shown in Fig. 1.1.4 [3].

![I-V Characteristics Diagram](image)

**Fig. 1.1.4** Typical DC I-V characteristics of an AlGaAs/GaAs HEMT: (a) output curve; (b) transfer curve.

Compared with conventional Si-based electronic devices, HEMTs have the following advantages listed in Table 1-1.

<table>
<thead>
<tr>
<th>Table 1-1 Advantages of the HEMT structure.</th>
</tr>
</thead>
<tbody>
<tr>
<td>• High electron mobility</td>
</tr>
<tr>
<td>• Small source resistance</td>
</tr>
<tr>
<td>• High $f_T$ due to high electron velocity in large electrical fields</td>
</tr>
<tr>
<td>• High transconductance due to small gate-to-channel separation</td>
</tr>
<tr>
<td>• High output resistance</td>
</tr>
</tbody>
</table>
After the introduction of the field-effect transistor in the early 1960s, equivalent circuit models were introduced and analyzed by many investigators. These models were modified after the emergence of GaAs MESFET. After the introduction of the heterostructure HEMTs with submicron gate lengths, these models were further modified and the most popular one is shown in Fig. 1.1.5 [6].

![Circuit Diagram]

\[ im = g_m V_g \exp(-j\omega t) \]

Fig. 1.1.5 Equivalent circuit model for a HEMT, the intrinsic circuit model is enclosed by the dashed line.

The equivalent circuit for the intrinsic HEMT is shown within the dashed rectangular boundary, which includes the gate capacitance \((C_g)\), the charging resistance \((r_i)\), the output conductance \((g_0)\), and the drain-to-gate transconductance \((g_m)\). The element \(C_i\) (not shown here), which arises due to the passive coupling between the drain and the channel conducting layer above \(r_i\) via the buffer-substrate region, is not included. These intrinsic parameters, together with the extrinsic ones, can be used to analysis and predict the AC operation behavior of the HEMT. They
can be extracted from the small-signal S-parameter measurements. The origins of these elements are shown in Fig. 1.1.6 [7].

![Diagram](image)

**Fig. 1.1.6** The physical origin of the elements in the equivalent circuit model of HEMT.

Combined with the parameter extraction techniques, the equivalent circuit can be used to characterize the performance of the devices. In the real applications, it is also desirable to predict the ultimate potential of the devices’ performance or make a decision which device should be chosen. Then, the first-order calculation of several performance figures of merit (FOMs) of the active devices will be very useful for making preliminary judgments. In most cases, the FOMs of interest include the current gain cutoff frequency (or cutoff frequency, $f_T$), power gain cutoff frequency (or maximum frequency of oscillation, $f_{max}$), output power density ($P_{out}$), power added efficiency (PAE), linear gain ($G_T$), minimum noise figure ($NF_{min}$), etc. These FOMs are only first-order indicators of the ultimate performance limit of the devices.
However, these data can be used as a basis of primary comparison between active devices.

As the frequency increases, the short-circuit current gain ($|h_{21}|$) of a HEMT device will decrease. The current gain cutoff frequency ($f_T$) of a HEMT device is the frequency when $|h_{21}|$ falls to unity. In the first order approximation, from the equivalent circuit shown in Fig. 1.1.5, $f_T$ can be driven as:

$$f_T = \frac{g_m}{2\pi C_g}$$

The FOM $f_T$ is an approximate criterion which can be used to compare the operation speed limitation of the devices. In general, the device with a high $f_T$ value usually can operate at higher frequencies than a device with a lower $f_T$ value. In the HEMT devices, $f_T$ can also be represented in term of the saturation drift velocity of the electrons in the 2DEG channel:

$$f_T = \frac{v_{sat}}{2\pi L_g},$$

where $v_{sat}$ is the saturation electron drift velocity and $L_g$ is the gate (channel) length. Obviously, higher electron velocity and smaller gate (channel) length will result in higher current gain cutoff frequency.

The power gain cutoff frequency, $f_{max}$, is the highest frequency at which power gain can be obtained from the device. That is, the power gain of the device is unity at $f_{max}$. As $f_T$, $f_{max}$ is an indicator of the ultimate operating frequency of the device. High $f_{max}$ value is desirable in high frequency applications. In microwave applications, where the power gain of the conjugately matched circuits are mostly concerned with,
$f_{\text{max}}$ attracts more interest from the designers than $f_T$ does. Usually, for simplification, in the definition of the power gain cutoff frequency, the power gain is the unilateral power gain (U), so $f_{\text{max}}$ is defined as the frequency at which U reaches unity. For HEMT devices, the unilateral gain can be represented in terms of the two-port $y$-parameters of the device:

$$U = \frac{|y_{21} - y_{12}|^2}{4[\text{Re}(y_{11}) * \text{Re}(y_{22}) + \text{Re}(y_{12}) * \text{Re}(y_{21})]}$$

The expression of $f_{\text{max}}$ can be extracted from the device equivalent circuit shown in Fig. 1.1.5. In the first-order approximation, $f_{\text{max}}$ can be written as [8]:

$$f_{\text{max}} = \frac{f_T}{2} \sqrt{\frac{R_{ds}}{R_i + R_g}},$$

where $R_i$ is the channel charging resistance, $R_g$ is the gate parasitic resistance, $R_{ds}$ is the output resistance, and $f_T$ is the current gain cutoff frequency. This equation provides some useful relationship between $f_T$ and $f_{\text{max}}$ when the device works at high frequency.

As mentioned previously, HEMT is a promising candidate for high frequency and high power applications due to its high carrier mobility and high current handling capability. The small-signal FOMs, $f_T$ and $f_{\text{max}}$, provide guidelines for the frequency performance of HEMTs, while to evaluate microwave large signal (or power) performance of them, some other FOMs should be considered. Two important large-signal FOMs are the output power density ($P_{\text{out}}$) and the power added efficiency (PAE). For class A operation, the theoretical maximum output power can be found out by:
\[ P_{out,\text{max}} = \frac{1}{2} (I_{\text{max}} - I_{\text{min}}) (V_{BR} - V_K), \]

where \( I_{\text{max}} \) is the maximum channel current, \( I_{\text{min}} \) is the minimum drain current due to the gate-drain and/or source-drain leakage, \( V_{BR} \) is the off-state breakdown voltage of the device, and \( V_K \) is the knee voltage. This approximate equation of the maximum output power is graphically presented in Fig. 1.1.7 [9], where the device is assumed to work along the ideal load line (a straight line) with an constant knee voltage and an adequate large-signal gain.

![Diagram of HEMT operation](image)

Fig. 1.1.7 Schematic representation of a HEMT operating in Class A.

The other important microwave large-signal FOM is the power added efficiency, PAE. For class A operation, the PAE of the device can be written in terms of the power gain as:

\[ PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}(1 - 1/G_a)}{P_{DC}} = \frac{1}{2} \left( 1 - \frac{1}{G_a} \right), \]
where $G_a$ is the power gain of the device. It can be found the maximum value of PAE for class A operation approaches 50% with infinite $G_a$. For class B operation, the PAE is higher, which has a maximum value of $\pi/4 \sim 78.5\%$.

1.2 AlGaN/GaN-based HEMTs

Due to their large band gap, high breakdown field, good thermal stability, and good electrons transport properties (with electron mobility up to 2000 cm$^2$/V-s and peak drift velocity of $1.2 \times 10^7$ cm/s at room temperature), GaN-based devices are becoming promising candidates for high voltage, high power and high frequency applications. III-nitrides, GaN, AlN, InN and their alloys, have a large covering range of band-gap values, which varies from 0.8 eV (InN) to 6.2 eV (AlN). Fig. 1.2.1 [10] shows the distribution of band-gap values of the hexagonal ($\alpha$-phase) GaN, AlN and InN versus their lattice constant ($a_0$).

![Fig. 1.2.1 Bandgap of hexagonal ($\alpha$-phase) InN, GaN and AlN versus lattice constant $a_0$.](image)

14
The lattice constants \( a_0 \) and \( c_0 \), bandgaps and binding energies of hexagonal InN, GaN and AlN are listed in Table 1-2 [10].

<table>
<thead>
<tr>
<th>Wurtzite 300 K</th>
<th>AlN</th>
<th>GaN</th>
<th>InN</th>
</tr>
</thead>
<tbody>
<tr>
<td>( a_0 ) (Å)(^a)</td>
<td>3.112</td>
<td>3.189</td>
<td>3.54</td>
</tr>
<tr>
<td>( c_0 ) (Å)(^a)</td>
<td>4.982</td>
<td>5.185</td>
<td>5.705</td>
</tr>
<tr>
<td>( c_0/a_0 ) (exp.)(^a)</td>
<td>1.6010</td>
<td>1.6259</td>
<td>1.6116</td>
</tr>
<tr>
<td>( c_0/a_0 ) (calc.)(^b)</td>
<td>1.6190</td>
<td>1.6336</td>
<td>1.6270</td>
</tr>
<tr>
<td>( u_0 )(^b)</td>
<td>0.380</td>
<td>0.376</td>
<td>0.377</td>
</tr>
<tr>
<td>( a_{\text{Bohr}} ) (Å)(^b)</td>
<td>5.814</td>
<td>6.04</td>
<td>6.66</td>
</tr>
<tr>
<td>( E_g(M-N))(^c) (eV)(^a)</td>
<td>2.88</td>
<td>2.20</td>
<td>1.98</td>
</tr>
</tbody>
</table>

\(^a\) From [11]  
\(^b\) From [12]  
\(^c\) \( M = \text{In, Ga or Al, N} = \text{Nitride} \)

As reported in [10], nitride-based semiconductors have a unique property compared to GaAs system, a very strong polarization field within the crystal. This polarization field has profound impacts on the electronic properties of GaN-based heterostructures. The polarization field in the nitride-based heterostructures comes from two parts, the spontaneous polarization and the piezoelectric polarization. Due to the non-central symmetry, nitrides exhibit a macroscopic spontaneous polarization field along the hexagonal c-axis in the wurtzite lattice. The values of spontaneous polarization field in nitrides are quite large, and of the same order of magnitude as in ferroelectric crystals. In addition, nitrides lack inversion symmetry and exhibit piezoelectric effects when strained along c-axis, the piezoelectric coefficients being
an order of magnitude larger than those in other traditional III-V semiconductors [13]. The direction of polarization field in nitrides depends on the polarity of the crystal, namely whether the cation sites or the anion sites of the crystal bi-layers are facing toward the sample surface [14]. In cation-face samples, the polarization field points away from the surface to the substrate. (Fig. 1.2.2, left) While in anion-face samples, the direction of polarization field is inverted (Fig. 1.2.2, right). Almost all MOCVD grown nitrides are of cation-face. Nitride alloys prepared by MBE are usually anion-face samples, yet one can invert the polarity by depositing a thin AlN buffer layer prior to the growth of GaN. With the assistance of the polarization field, a polarization charge density of $10^{13}$ cm$^{-2}$ can be achieved in a strained-Al$_{0.3}$Ga$_{0.7}$N/relaxed-GaN system [15].

![Ga-face and N-face](image)

**Fig. 1.2.2** Crystal structure of the Ga-face (left) and N-face (right) wurtzite GaN.

Compared with AlGaAs/GaAs HEMTs, the origin of the 2DEG in AlGaN/GaN HEMTs is quite different. Due to the strong polarization field in the AlGaN/GaN heterostructure, a 2DEG with much higher density ($\sim 10^{13}$ cm$^{-2}$) can be achieved
without modulation doping [16]. With an undoped AlGaN barrier and GaN channel layer, what should be the source of the electrons in the 2DEG channel? If the electrons come from the GaN buffer, the buffer layer will be positively charged and no potential well can be formed at the AlGaN/GaN hetero-interface. By the studies of Ibbetson et al. [17], the surface states serve as the source of the electrons in the 2DEG channel. With the electrostatic field induced by the polarization field in AlGaN/GaN heterostructure, the band profile and the electron distribution are modified and a large number of electrons transfer from the surface states to the AlGaN/GaN hetero-interface, forming a 2DEG with a density of \( \sim 10^{13} \text{ cm}^2 \). The mechanism of the contribution of surface states to 2DEG in AlGaN/GaN heterostructure is shown in Fig. 1.2.3.

![Diagram](image)

Fig. 1.2.3 Band profiles of the AlGaN/GaN heterostructures with different AlGaN thicknesses, which demonstrates the surface states’ contribution to the 2DEG formation.

Due to the advantages of the GaN-based heterostructures, tremendous progress has been made in the development of AlGaN/GaN HEMT since it was firstly demonstrated by Khan et al. in 1993 [18]. Many works have been done to improve
the material quality and device performances of GaN HEMTs. Table 1-3 lists the most representative developments of GaN HEMTs.

Table 1-3 Historical Development of GaN-based HEMTs.

<table>
<thead>
<tr>
<th>Year</th>
<th>Event</th>
<th>Authors</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1969</td>
<td>GaN by hydride vapor phase epitaxy</td>
<td>Maruska and Tietjen</td>
<td>[19]</td>
</tr>
<tr>
<td>1971</td>
<td>GaN by MOCVD</td>
<td>Manasevit et al.</td>
<td>[20]</td>
</tr>
<tr>
<td>1992</td>
<td>AlGaN/GaN two-dimensional electron gas</td>
<td>Khan et al.</td>
<td>[21]</td>
</tr>
<tr>
<td>1993</td>
<td>AlGaN/GaN HEMT</td>
<td>Khan et al.</td>
<td>[18]</td>
</tr>
<tr>
<td>1994</td>
<td>Microwave AlGaN/GaN HFET</td>
<td>Khan et al.</td>
<td>[22]</td>
</tr>
<tr>
<td>1996</td>
<td>Microwave power AlGaN/GaN MODFET</td>
<td>Wu et al.</td>
<td>[23]</td>
</tr>
<tr>
<td>1998</td>
<td>Reveal current compression in GaN MODFET</td>
<td>Kohn et al.</td>
<td>[24]</td>
</tr>
<tr>
<td>1999</td>
<td>6.9 W/mm @ 10 GHz GaN HEMT on SiC</td>
<td>Sheppard et al.</td>
<td>[25]</td>
</tr>
<tr>
<td>2000</td>
<td>Surface passivated AlGaN/GaN HEMTs</td>
<td>Green et al.</td>
<td>[26]</td>
</tr>
<tr>
<td>2004</td>
<td>30 W/mm @ 8 GHz GaN HEMT with field plate</td>
<td>Wu et al.</td>
<td>[27]</td>
</tr>
</tbody>
</table>

As mentioned above, the most promising application for GaN-based HEMTs is high power devices. The competitive advantages of GaN devices and amplifiers for a commercial product are described in Table 1-4 [28]. The first column states the required performance benchmarks for any technology for power devices and the second column lists the enabling feature of GaN-based devices that fulfill this need. The last column summarizes the resulting performance advantages at the system level and to the customer. The highlighted features offer the most significant product benefits.

The rate of progress in the power density and total power available form AlGaN/GaN HEMTs has been remarkable, as shown in Fig. 1.2.4 [28].
Table 1-4 Competitive advantages of GaN devices

<table>
<thead>
<tr>
<th>Need</th>
<th>Enabling Feature</th>
<th>Performance Advantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Power Density</td>
<td>Wide Bandgap, High Field</td>
<td>Compact, Ease of Matching</td>
</tr>
<tr>
<td>High Voltage Operation</td>
<td>High Breakdown Field</td>
<td>Eliminate/Reduce Step Down</td>
</tr>
<tr>
<td>High Linearity</td>
<td>HEMT Topology</td>
<td>Optimum Band Allocation</td>
</tr>
<tr>
<td>High Frequency</td>
<td>High Electron Velocity</td>
<td>Bandwidth, m-Wave/mm-wave</td>
</tr>
<tr>
<td>High Efficiency</td>
<td>High Operating Voltage</td>
<td>Power Saving, Reduced Cooling</td>
</tr>
<tr>
<td>Low Noise</td>
<td>High Gain, High Velocity</td>
<td>High Dynamic Range receivers</td>
</tr>
<tr>
<td>High Temperature Operation</td>
<td>Wide Bandgap</td>
<td>Rugged, Reliable, Reduced</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Cooling</td>
</tr>
<tr>
<td>Thermal Management</td>
<td>SIC-Substrate</td>
<td>High Power Devices with</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reduced Cooling Needs</td>
</tr>
<tr>
<td>Technology Leverage</td>
<td>Direct Bandgap:</td>
<td>Driving Force for Technology:</td>
</tr>
<tr>
<td></td>
<td>Enable for Lighting</td>
<td>Low Cost</td>
</tr>
</tbody>
</table>

Fig. 1.2.4 Historical progress in GaN transistor technology: (a) Power density of AlGaN/GaN HEMTs versus year; (b) Total Power of AlGaN/GaN HEMTs versus year.
GaN HEMTs have demonstrated one-order higher power density and higher efficiency over the conventional Si- and GaAs-based RF and microwave transistors. This features a more compact size in power amplifiers using GaN-based devices than conventional devices.

1.3 Limitations in the Conventional AlGaN/GaN HEMTs

1.3.1 Linearity Limitation

The unique advantages of the GaN-based HEMTs make them suitable for high frequency, high power microwave applications. One of the most promising applications is the power amplifiers in 3G wireless communication systems, such as WCDMA/UMTS. Because of the large dynamic range in the variable envelope of the modulation signals, stringent requirements of linearity are imposed on the power amplifiers used in these systems. As a result, recently, there have been intensive activities in characterizing the linearity of conventional AlGaN/GaN HEMT [29]-[32] and metal-oxide-semiconductor (MOS) field-effect transistors [33]. It has been shown that conventional AlGaN/GaN HEMTs require advanced linearization techniques such as digital pre-distortion to satisfy the adjacent channel power ratio (ACPR) requirement for W-CDMA standard. One undesirable feature with regard to the linearity is the significant reduction of transconductance ($G_m$) and gain at high current levels [27]. Fig. 1.3.1(a) shows the schematic transfer curve and transconductance of a conventional AlGaN/GaN HEMT. At high current levels, the
transconductance decreases quickly with the increase of gate bias. This feature is undesirable in the application of high power microwave power amplifiers which operate with large-dynamic-range signals. Signals go through the transistor will be distorted and errors will be induced, as shown in Fig. 1.3.1(b).

![Graphs showing transconductance and output voltage](image)

**Fig. 1.3.1** (a) Typical transfer and transconductance characteristics of a conventional AlGaN/GaN HEMT; (b) Distortion in the output signal due to the non-linear $G_m$ at high current levels.

Some groups are investigating ways of improving the linearity by using field-plate [34] and modifying the access resistance [35]. Most of these works focus on the device fabrication technologies or the AlGaN barrier layer. Following the development of GaAs-based HEMTs, one possible way to effectively improve the electronic characteristics of the AlGaN/GaN HEMTs is to optimize the epitaxial structure. In our work, we will focus on the channel region of the AlGaN/GaN HEMT structure and try to improve its linearity performance by modifying the band profile. The details will be covered in Chapter 2.
1.3.2 Limitation of Carrier Confinement

One of the most important criteria for judging the performance of AlGaN/GaN HEMTs is the buffer isolation behavior. In the conventional AlGaN/GaN HEMT structure, the 2DEG channel is located in the GaN channel layer, which is directly on the top of GaN buffer layer. Due to the homogeneous characteristic of the GaN channel and buffer layers, the conduction band below the AlGaN barrier is continuous and rises slowly with the depth, as shown in Fig. 1.3.2. This relatively flat conduction band profile results in an intrinsic drawback of the conventional AlGaN/GaN HEMTs: the carriers in the 2DEG channel cannot be confined so well, some of them spill over to the buffer, which results in poor buffer isolation and larger leakage current. 2DEG in the channel may also get its mobility degraded due to its poor confinement.

Fig. 1.3.2 Schematic conduction band profile of the conventional AlGaN/GaN HEMTs, with some carriers spill over to buffer.

Many works have been carried out by some groups. For example, Fe-doped GaN buffer [34] was tried to achieve better isolation, AlGaN/GaN/AlGaN/GaN double-heterostructure HEMT [36] was proposed to improve the carrier confinement by
replacing GaN buffer layer with AlGaN, AlGaN/InGaN/GaN HEMTs [37] were reported with improved isolation due to an InGaN channel layer. Although these works can improve the buffer isolation, the overall performances of the device were suffered. In our work, some novel HEMT structure with modified band profile for better carrier confinement and negligible performance degradation was designed, which will be described in Chapter 3.

1.4 Objective of This Work

To overcome the two major limitations in the conventional AlGaN/GaN HEMTs, the objective of this work is to design optimized ex pitaxial AlGaN/GaN HEMT structures with improved linearity and carrier confinement characteristics. The optimization works are focused on the channel part, which is a crucial part in the AlGaN/GaN-based HEMTs but has not been explored frequently yet.

Chapter 2 focus on the design and optimization of an Al$_x$Ga$_{1-x}$N/Al$_y$Ga$_{1-y}$N/GaN composite-channel HEMT (CC-HEMT) structure with improved linearity feature by employing an Al$_y$Ga$_{1-y}$N layer as the channel material. DC and bias-dependent RF small-signal characteristics of the CC-HEMTs are demonstrated in detail, followed by the large signal power and linearity characteristics. The details of device fabrication will also be covered in Chapter 2.

Chapter 3 covers the design, fabrication, characterization of an Al$_x$Ga$_{1-x}$N/GaN/In$_y$Ga$_{1-y}$N/GaN double-heterojunction HEMT (DH-HEMT) structure which
features a thin InGaN notch layer to achieve improved carrier confinement. Detailed DC, RF small-signal and large-signal characteristics of the device fabricated on this newly-developed DH-HEMT structure are described.

Chapter 4 contains the works of GaN-based enhancement-mode (E-mode) HEMTs fabricated on the optimized InGaN-notch DH-HEMT structure by employing a fluoride-based plasma treatment technique. The large-signal power performance and noise characteristics of E-mode HEMTs are reported for the first time.

Finally, the work is summarized in Chapter 5, and suggestions for the future work are also provided.
CHAPTER 2

**ALₓGA₁₋ₓN/ALᵧGA₁₋ᵧN/GaN COMPOSITE-CHANNEL HEMTS (CC-HEMTS) WITH ENHANCED LINEARITY**

2.1 Channel Engineering for Enhanced Linearity in GaN-based HEMTs

As mentioned in Chapter 1, the linearity of the conventional HEMTs suffers from the $G_m$ compression at high current levels, which is an undesired feature for the application with large signal dynamic range. One possible dominant factor of the $G_m$ and gain compression at high current levels is the large transverse electric-field ($E_f$-field) perpendicular to the channel at the hetero-interface. Due to the large conduction band offset between AlGaN and GaN, a large transverse E-field ($E_T$) is induced at AlGaN/GaN hetero-interface, as shown in Fig. 2.1.1.

![Diagram](image)

Fig. 2.1.1 Schematic conduction band profile ($E_C$) and the transverse electrical-field ($E_T$) distribution in the conventional AlGaN/GaN system.

This strong $E_T$ pushes the 2DEG closer to the hetero-interface when the electrons transport laterally from source to drain, and then enhances the scattering of the
electrons, especially with high gate bias. The severe scattering degrades the electron mobility [38], results in the reductions in $G_m$ and gain. Based on this mechanism, to suppress the compression of $G_m$ and gain, one possible solution is to modify the band profile near the AlGaN/GaN hetero-interface to achieve a lower $E_T$ and then alleviate the scattering. That is, a new AlGaN/GaN-based epitaxial structure with decreased $E_T$ should be employed for the purpose of enhanced linearity.

By investigation, it is found the transverse E-field in the AlGaN/GaN HEMT structure is caused by the discontinuity between the AlGaN barrier and GaN channel layer. To reduce this E-field, the channel, which is GaN in the conventional AlGaN/GaN HEMT structure, should be replaced by some other material which has smaller conduction band offset at the hetero-interface and then reduces the built-in $E_T$, as shown in Fig. 2.1.2 (b). By this kind of “channel-engineering” work, novel HEMT structures can be designed for enhanced performances in different issues.

One natural option of the channel material in this new HEMT structure is AlGaN with lower aluminum composition than the barrier. That is, an Al$_x$Ga$_{1-x}$N/Al$_y$Ga$_{1-y}$N/GaN (x > y) HEMT structure is supposed to exhibit lower $E_T$ at the hetero-interface than its conventional counterpart. An AlGaN layer with low aluminum composition can provide lower polarization charge density and is easy to be integrated into the growth procedure of the conventional AlGaN/GaN.
Fig. 2.1.2 Band profiles and transverse electrical filed \( (E_T) \) distribution in (a) the conventional AlGaN/GaN HEMT and (b) the desired HEMT structure which employs a different channel material.

Fig. 2.1.3 shows the schematic band profile of an \( Al_xGa_{1-x}N/Al_yGa_{1-y}N/GaN \) (\( x > y \)) HEMT structure. Due to the conduction band discontinuity, there will be two hetero-interfaces. The upper one is between the barrier and the channel layer, the lower one is between the channel layer and the buffer. These two hetero-interfaces result in two 2DEG channels. It is supposed that most electrons are located in the upper channel (major channel), while the lower channel only accommodates a few electrons (minor channel). Meanwhile, the barrier height at the lower hetero-interface should be lower enough to ensure a strong coupling between the two channels to avoid two \( G_m \) peaks. The electrons in the minor channel can compensate the reduction of carrier density in the major channel due to the lower polarization charge.
density provided by an Al$_y$Ga$_{1-y}$N channel layer. Based on this mechanism, we named this Al$_x$Ga$_{1-x}$N/Al$_y$Ga$_{1-y}$N/GaN HEMT structure a “Composite-Channel HEMT” (CC-HEMT) [39], [40], [D10]. This is the reason why we choose this CC-HEMT structure instead of another one which has an AlGaN barrier with lower aluminum composition, which has lower carrier concentration.

![Schematic band profile carrier distribution of an Al$_x$Ga$_{1-x}$N/Al$_y$Ga$_{1-y}$N/GaN (x > y) HEMT structure.](image)

2.2 Design of the Al$_x$Ga$_{1-x}$N/Al$_y$Ga$_{1-y}$N/GaN CC-HEMTs

From the analysis in the previous section, an Al$_x$Ga$_{1-x}$N/Al$_y$Ga$_{1-y}$N/GaN composite-channel HEMT (CC-HEMT) structure will be suitable for reduced $E_T$ and then improve devices’ $G_m$ linearity. To find out the optimum epitaxial structure
which can enhance the linearity and minimize other undesirable performance degradations, several structure parameters should be designed carefully.

In our work, by focusing the channel part, the barrier AlGaN layer, which has been optimized in our conventional HEMTs, will be kept unchanged in this $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{Al}_y\text{Ga}_{1-y}\text{N}/\text{GaN}$ structure.

Two important parameters of the $\text{Al}_y\text{Ga}_{1-y}\text{N}$ should be optimized, the aluminum composition ($y$) and the channel layer thickness ($d$). The aluminum composition of the $\text{Al}_y\text{Ga}_{1-y}\text{N}$ determines the polarization charge density which affects the $E_T$ at the $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{Al}_y\text{Ga}_{1-y}\text{N}$ hetero-interface. To achieve a lower $E_T$ that can alleviate $G_m$ compression, a high aluminum composition is preferred, that is, the larger $y$ is, the better $G_m$ linearity can be obtained. However, the electron transport of AlGaN decreases with the increase of aluminum composition. At same time, the reduction of the transverse electrical field is accompanied with a lower polarization charge density, which will result in a small carrier density in the major 2DEG channel. So, too high an aluminum composition will degrade the overall performance of the device. Then, a trade-off between the transverse electrical field and the carrier concentration should be made for enhancement of the overall performance.

To get some guidance for the aluminum composition in our design and avoid unnecessary attempts in the final material growth work, some first-order calculations were done. By solving Poisson's equation and the Fermi-Dirac statistics, we calculated the conduction band profiles of the CC-HEMT structures with different aluminum compositions, which are shown in Fig. 2.2.1, together with the band
profile of the conventional EHMT structure for comparison. In the calculation, the barrier layer is fixed same as the conventional HEMTs, which will be described in the latter part of this chapter, and the thickness of the Al$_y$Ga$_{1-y}$N channel layer is fixed to be 10 nm. With the increase of the aluminum composition in the Al$_y$Ga$_{1-y}$N channel layer, the depth of the minor channel increases, resulting in higher carrier concentration in it. With an aluminum composition of 10% and 15%, the minor channel is deep enough to accommodate a large number of electrons. At same time, the barrier height at lower hetero-interface is large enough to separate the two channels completely.

![Diagram](image)

**Fig. 2.2.1** Calculated band profiles of the CC-HEMTs with different aluminum compositions and the conventional HEMTs.

The transverse electrical field ($E_T$) distributions are also calculated and the results are plotted in Fig. 2.2.2. It can be found that the aluminum composition of the Al$_y$Ga$_{1-y}$N channel layer does affect the peak value of $E_T$ at the Al$_y$Ga$_{1-y}$N/Al$_y$Ga$_{1-y}$N hetero-interface, higher aluminum composition leads to lower peak $E_T$ value.
Fig. 2.2.2 Calculated transverse electrical field distributions of the CC-HEMTs with different aluminum compositions and the conventional HEMTs.

To find out how much the reduced polarization charge can affect the carrier concentration in the major channel, the carrier distribution profiles of these structures are calculated and plotted in Fig. 2.2.3. It can be found that with an aluminum composition of 10% in the Al_{x}Ga_{1-x}N channel layer, the peak carrier concentration in the major channel decrease a lot, only about 60% of the value in the conventional one. For an aluminum composition of 15%, the reduction can be large as 65%. At the same time, it will result a large number of carriers in the minor channel, which is unwanted because it will cause two $G_{m}$ peaks just as the double-channel HEMTs [D2] and degrades the linearity. Following these calculation results, an aluminum composition of 5% is fixed in the preliminary design to ensure an acceptable carrier density reduction in the major channel and no well-defined 2DEG channel at the Al_{x}Ga_{1-x}N/GaN hetero-interface.
Fig. 2.2.3 Calculated carrier distributions of the CC-HEMTs with different aluminum compositions and the conventional HEMTs.

After the decision of the aluminum composition of the Al$_x$Ga$_{1-x}$N channel, the other key parameter, the thickness of the channel layer, should be optimized. The channel layer thickness determines the separation between the two channels and the depth of the minor channel. A series of CC-HEMT structures with different channel layer thicknesses were designed for the growth and the subsequent device fabrication. Three thicknesses were tried: 3 nm, 6 nm, and 9 nm in the first batch of samples. Before the growth of these samples, the calculations of band profile, transverse electrical field distribution, and carrier distribution were also carried out and the results are plotted in Fig. 2.2.4. From the figures it can be found that the CC-HEMT with an 3-nm-thick AlGaN channel layer has a minor channel totally below the Fermi level, while for the CC-HEMT with a thickness of 9 nm, the minor channel is well separated from the major one by the barrier at the Al$_x$Ga$_{1-x}$N/GaN hetero-interface. The different features of the minor channel in these structures will affect
the screen effect of the minor channel on the buffer and then the large signal performance, which will be discussed in the latter parts. One the other hand, as shown in Fig. 2.2.4 (b) and (c), the $E_T$ and the carrier concentration at the $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ hetero-interface, which are dominated by the polarization charge, are same in these three structures with same aluminum composition.
Fig. 2.2.4 Calculated (a) band profiles, (b) $E_T$ distributions, and (c) carrier distributions of the CC-HEMTs with different InGaN layer thickness and the conventional HEMTs.

2.3 Material Growth and Device Fabrication

2.3.1 $Al_{0.3}Ga_{0.7}N/Al_{0.05}Ga_{0.95}N/GaN$ CC-HEMTs Growth

The $Al_{0.3}Ga_{0.7}N/Al_{0.05}Ga_{0.95}N/GaN$ CC-HEMT structures, with the schematic cross section shown in Fig. 2.3.1, were grown on $c$-plane sapphire substrates in an Aixtron AIX 2000 HT MOCVD system. After initial desorption at 1200 $^\circ$C, a GaN nucleation layer was grown at 550 $^\circ$C, followed by a 2.5-$\mu$m-thick unintentionally doped GaN buffer layer. Then the layer which provides the major channel, an undoped $Al_{0.05}Ga_{0.95}N$ layer with different thicknesses, 3 nm (structure A), 6 nm (structure B), and 9 nm (structure C), was grown followed by the AlGaN barrier layer with 30% Al composition. The barrier layers for all of these samples are
identical, which consist of a 3-nm-thick undoped spacer, a n-doped \((2 \times 10^{18} \text{ cm}^{-3})\) 21-nm-thick carrier supplier layer, and a 2-nm-thick undoped cap layer.

![Schematic cross-section of the Al\(_{0.3}\)Ga\(_{0.7}\)N/Al\(_{0.05}\)Ga\(_{0.95}\)N/GaN CC-HEMT device.]

Hall measurements were conducted on these samples at room temperature through a Hall Bridge pattern fabricated on the sample, whose layout is shown in Fig. 2.3.2. The measuring results of the Hall mobility, carrier densities and sheet resistances are listed in Table 2-1.

![Layout of the Hall Bridge for Hall measurements.]

35
Table 2-1 Hall measurement results of the CC-HEMT structures.

<table>
<thead>
<tr>
<th>Structure</th>
<th>Hall Mobility (cm²/Vs)</th>
<th>Carrier Density (x10¹⁵ cm⁻²)</th>
<th>Sheet Resistance (Ω/sq)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td>1150</td>
<td>1.4</td>
<td>420</td>
</tr>
<tr>
<td>A (3 nm)</td>
<td>1040</td>
<td>1.35</td>
<td>480</td>
</tr>
<tr>
<td>B (6 nm)</td>
<td>980</td>
<td>1.25</td>
<td>550</td>
</tr>
<tr>
<td>C (9 nm)</td>
<td>940</td>
<td>1.2</td>
<td>600</td>
</tr>
</tbody>
</table>

To profile the carrier distribution in the CC-HEMTs, capacitance-voltage (C-V) measurement was carried out on a Schottky diode with Schottky contact formed on the top of Al₅Ga₅₋ₓN barrier and the ohmic contact to the channel serving as the other electrode, as shown in Fig. 2.3.3.

Fig. 2.3.3 Schottky diode fabricated of wafer for C-V measurement.

By applying a small AC signal on the DC-biased Schottky contact, the differential capacitance of the diode can be measured. The differential capacitance of the depletion layer is:

\[
C = \frac{dQ}{dV}
\]  

(2.1)

The charge in the depletion layer is:
\[ Q = qN_B W = A q N_B \sqrt{\frac{2 \varepsilon}{q N_B}} \left( V_{bi} \pm V - \frac{2 k_B T}{q} \right) = A \sqrt{2 \varepsilon q N_B \left( V_{bi} \pm V - \frac{2 k_B T}{q} \right)} \]  

(2.2)

Where \( A \) is the area of the depletion layer, \( W \) is the thickness of the depletion layer, \( N_B \) is the carrier density, \( V_{bi} \) is the build-in potential, \( V \) is the applied DC bias, \( k_B \) is Boltzmann’s constant, \( T \) is the absolute temperature, and \( q \) is the charge of electron.

Applying (2.2) to (2.1), the capacitance can be written as:

\[ C = A \sqrt{\frac{\varepsilon q N_B}{2}} \left( V_{bi} \pm V - \frac{2 k_B T}{q} \right)^{-1/2} \]  

(2.3)

Then,

\[ \frac{1}{C^2} = \frac{2}{\varepsilon q N_B} \left( V_{bi} \pm V - \frac{2 k_B T}{q} \right) \]  

(2.4)

In an AlGaN/GaN heterostructure, the carrier density \( N_B \) is a function of depth:

\[ N_B = N_B(x) \]  

By differentiating (2.4), we can get:

\[ \frac{d}{dV} \left( \frac{1}{C^2} \right) = \frac{2}{\varepsilon q N_B(x)} \]  

(2.5)

Then the carrier density can be written as:

\[ N_B(x) = \frac{2}{q \varepsilon} \frac{1}{d \left( \frac{1}{C^2} \right)} = \frac{C^3}{q \varepsilon \frac{dC}{dV}} \]  

(2.6)

And the depth can be written as:

\[ x = W = \frac{\varepsilon}{C} \]  

(2.7)

Now, by using (2.6) and (2.7), the carrier density distribution along the depth can be found out through bias-dependent C-V measurement.

The carrier distribution profiles along with the C-V characteristics are plotted in Fig. 2.3.4. It can be found that for structure A, the two channels couple with each
other strongly, the C-V curve is very sharp and only one peak can be observed in the
carrier distribution profile. For structure B, the C-V curve is not sharp and structure
A, and a very small secondary peak can be found in the carrier distribution profile.
When the channel thickness increases to 9 nm, a secondary shoulder appeared in the
C-V curve and clear minor peak can be found in the carrier distribution. This is due
to the larger space between the two channels and the larger barrier height at the
$\text{Al}_{0.05}\text{Ga}_{0.95}\text{N}/\text{GaN}$ hetero-interface above the Fermi level, which reduced the
coupling effect.

![C-V curves and the extracted carrier distribution profiles of three CC-
HEMT structures with different channel thicknesses.](image)

Fig. 2.3.4 C-V curves and the extracted carrier distribution profiles of three CC- 
HEMT structures with different channel thicknesses.

### 2.3.2 $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{Al}_y\text{Ga}_{1-y}\text{N}/\text{GaN}$ CC-HEMT Device Fabrication

The grown $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{Al}_y\text{Ga}_{1-y}\text{N}/\text{GaN}$ CC-HEMT epilayers were used to
fabricate devices. Device active regions were defined using 300-nm-thick mesa
etching by $\text{Cl}_2$-based inductively coupled plasma reactive ion etching (ICP-RIE). It is
followed by the source/drain ohmic contacts formation by a rapid thermal annealing of e-beam evaporated Ti/Al/Ni/Au multilayer at 850 °C for 30 seconds. Using on-wafer transfer length method (TLM) patterns, the ohmic contact resistance was typically measured to be 1.0 ohm-mm for all the samples. Gate electrodes with 1 μm length were then defined by contact photolithography, Ni/Au e-beam evaporation and lift-off, subsequently. The devices have a source-gate spacing of $L_{sg} = 1 \mu$m and a gate-drain spacing of $L_{gd} = 1 \mu$m. Finally, plasma enhance chemical vapor deposition (PECVD) was used to deposit SiN for device passivation. The layout for the device fabrication is shown in Fig. 2.3.5, where the metal pad for source, drain and gate electrode contacts are deposited simultaneously with the gate figure. The flow of the fabrication process of AlGaN/GaN-based HEMTs is shown in Fig. 2.3.6 and more details can be found in Appendix A.

![Fig. 2.3.5 Layout for the AlGaN/GaN-based HEMTs fabrication.](image-url)
Fig. 2.3.6 Process flow of AlGaN/GaN-based HEMTs fabrication.
Fig. 2.3.7 shows the microscopy photos of the overall and zoom-in views of the HEMT devices we fabricated.

Fig. 2.3.7 Microscopy photos of the fabricated HEMT devices: (a) overall view; and (b) zoom-in view of the active region.

2.4 Device Characteristics

2.4.1 DC Characteristics

In our work, to characterize the DC characteristics of the HEMTs, we performed the measurements on the device with a gate dimension of 1 μm × 10 μm. The reason to choose this kind of small device is mainly due to the heating effect of the devices. Too wide a gate width will cause a severe DC performance degradation, which cannot be used to evaluate the real potential of the devices. Fig. 2.4.1 shows the layout and microscopy of this kind of small devices for DC characterizations. Differing from the standard devices shown previously, there are only three (instead of four) terminals in these small devices.
Fig. 2.4.1 (a) Layout and (b) microscopy photo of the small device for DC characterizations.

The typical DC $I_{DS}-V_{DS}$, $I_{DS}-V_{GS}$ and $G_m-V_{GS}$ characteristics of a $1 \mu m \times 10 \mu m$ device fabricated on three different CC-HEMT structures are plotted in Fig. 2.4.2.

Fig. 2.4.2 DC $I_{DS}-V_{GS}$ and $G_m-V_{GS}$ characteristics: (a) conventional HEMT; (b) structure A (CC-HEMT); (c) structure B (CC-HEMT); (d) structure C (CC-HEMT).
All the three CC-HEMT structures show similar DC characteristics, with a pinch-off voltage of about -5.5 V. The maximum drain current of the CC-HEMT structures is around 800 mA/mm with a gate bias of +1 V, which is a little bit lower than their conventional counterpart (~900 mA/mm), and the maximum $G_m$ is about 150~160 mS/mm, slightly lower than 175 mS/mm, the value achieved in the conventional one. This indicates that the inserted low Al composition AlGaN layer only results in small degree of mobility degradation and carrier density reduction. It can be found in Fig. 3 that the most important feature in the CC-HEMTs is that the $G_m$ is quite flat after the onset and remains close to its peak value at high current levels. On other words, the CC-HEMTs showed an improved linearity than the conventional AlGaN/GaN HEMTs.

Detailed DC $G_m$ characteristic parameters of these three CC-HEMT structures are summarized in Table 2-2, together with the values of our conventional HEMT structure. It can be found that at the maximum drain current ($V_{GS} = 1$ V), $G_m$ of about 120 mS/mm was obtained on these CC-HEMT structures, a drop of 21~24% from its peak value, which is much lower than that of conventional HEMT (44%). As mentioned above, this is a desirable feature. The flat $G_m$ leads to flat gain (and cutoff frequencies) over the full current operating range.

From the DC performances, it was found that the linearity performance, in terms of the $G_m$ compression at high current levels, were similar for the three CC-HEMT structures, which is much better than the conventional one.
Table 2-2 $G_m$ characteristics of the CC-HEMT and conventional HEMT devices.

<table>
<thead>
<tr>
<th>Structure</th>
<th>Peak $G_m$ (mS/mm)</th>
<th>$G_m$ @ $V_{GS}=1V$ (mS/mm)</th>
<th>$G_m$ Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td>175</td>
<td>98</td>
<td>44%</td>
</tr>
<tr>
<td>A (3 nm)</td>
<td>151</td>
<td>119</td>
<td>21%</td>
</tr>
<tr>
<td>B (6 nm)</td>
<td>159</td>
<td>121</td>
<td>24%</td>
</tr>
<tr>
<td>C (9 nm)</td>
<td>150</td>
<td>117</td>
<td>22%</td>
</tr>
</tbody>
</table>

There are some claims that the reduction of $G_m$ and $f_T$ at high current levels (or high gate bias voltages) is caused by the gate-bias-modulated source access resistance ($R_S$), which increases with the gate bias ($V_{GS}$) [41], [42]. To evaluate the influence of $R_S$ to the $G_m$ linearity, gated-TLM measurements were carried out to find out the relationship between $R_S$ and $V_{GS}$. A set of TLM pattern which includes gate fingers with different lengths was used for the measurements, as shown in Fig. 2.4.3.

Fig. 2.4.3 Layout of gated-TLM pattern for the extraction of source access resistance.

By applying a DC bias voltage between two neighboring TLM pads, the whole resistance can be divided into three parts, source access resistance $R_S$, channel
resistance \( R_{CH} \), and drain access resistance \( R_D \), as shown in Fig. 2.4.4. All of these three resistances are gate-bias-dependent.

![Diagram of resistance components](image)

Fig. 2.4.4 The separated contributions to the resistance between two TLM pads.

To extract the source access resistance, a very small DC voltage VDD (5 mV) was applied. With such a small bias voltage, the source access resistance and the drain access resistance were almost same, that is, \( R_s \approx R_d \). With different gate lengths, the sum of \( R_S \) and \( R_D \) (\( = 2R_S \)) can be extracted by extrapolating to the zero gate length.

The gate-bias-dependent source access resistance extracted from the gated-TLM measurements via the method mentioned above is shown in Fig. 2.4.5(a). It can be found that with the gate bias increases from near the threshold voltage, \( R_S \) decreases quickly at first and then approaches to a constant value. This result is different from the one reported in [41] and [42], where \( R_S \) increased with gate bias, as shown in Fig. 2.4.6. From the bias-dependent source access resistance curve extracted from the gated-TLM measurements, the gate bias modulation on \( R_S \) at high current levels is weak and can hardly affect the linearity of the device. The gate-bias-dependent channel resistance of the device is also extracted and the result is shown in Fig.
2.4.5(b). With the gate bias increases, the channel resistance reduces, which is caused by higher carrier density in the 2DEG channel at higher gate bias.

![Graph showing source access resistance (RS) and channel resistance (RCH)](image)

Fig. 2.4.5 Gate-bias-dependent (a) source access resistance (RS) and (b) channel resistance (RCH), extracted via gated-TLM measurements.

![Graph showing gate-bias-dependent source access resistance](image)

Fig. 2.4.6 Gate-bias-dependent source access resistance obtained in ref [41].

2.4.2 RF Small-Signal Characteristics

Full bias-range on-wafer small signal S-parameters measurements were conducted on 1 μm x 100 μm CC-HEMT devices fabricated on structure B (6-nm-thick Al0.05Ga0.95N layer), using a HP 4142B modular DC source/monitor and an Agilent 8722ES network analyzer with Cascade microwave probes. The reason we
focused on the CC-HEMT structure which features a 6-nm-thick Al$_{0.05}$Ga$_{0.95}$N layer is based on the combination of simulation results (please refer to section 2.2) and the power performance which will be discussed in the later section. This structure performs the best balance between the $G_m$ linearity and the other performances.

The full bias-range RF small signal transconductances were extracted from the S-parameters measured at 2 GHz from the equivalent small-signal circuit of HEMT device [6] shown in Fig. 2.4.7 and the result is plotted in Fig. 2.4.8. The details of the parameters’ extraction can be found in Appendix C.

\[ im = g_m V_d \exp(-j\omega t) \]

Fig. 2.4.7 Equivalent small-signal circuit model for AlGaN/GaN HEMTs.

Fig. 2.4.8 Bias-dependent $G_m$ curve extracted from on-wafer S-parameter measurements ($f = 2$ GHz) for 1 $\mu$m $\times$ 100 $\mu$m CC-HEMT device (structure B).
It was found that the AC transconductance of CC-HEMT presented a relatively flat profile in the whole operating bias range, which is an indication of good linearity. The peak value of AC transconductance is about 155 mS/mm, very close to the DC value. So there is no DC-to-AC dispersion of the transconductance on this CC-HEMT.

The full bias-range current gain and power gain cutoff frequencies, $f_T$ and $f_{max}$, were also extracted from the measured S-parameters and plotted in Fig. 2.4.9. All these parameters show much smaller bias dependence than their conventional counterparts. To make a more clear comparison, the $f_T, f_{max}$ versus $V_{gs}$ curves of the CC-HEMT and conventional HEMT are plotted together, as shown in Fig. 2.4.10. Relatively flat $f_T$ and $f_{max}$ were obtained for CC-HEMT from low to high current levels, while the conventional HEMT shows significant drop at high current levels.

Fig. 2.4.9 Bias-dependent cutoff frequencies for 1 μm × 100 μm CC-HEMT device (structure B): (a) $f_T$ and (b) $f_{max}$.
Fig. 2.4.10 Gate-bias dependent cutoff frequencies ($f_T$ and $f_{max}$) for 1 $\mu$m x 100 $\mu$m CC-HEMT (structure B) with a drain bias of 10 V.

More device parameters were extracted from the measured S-parameter. The full bias-range $C_{gs}$ and $C_{gd}$ at 2 GHz are plotted in Fig. 2.4.11. In the whole operating bias range of the device, both $C_{gs}$ and $C_{gd}$ show a relatively flat profile. The sum of these two parasitic capacitances is plotted in Fig. 2.4.12, which is quite flat in the operating bias range. Due to the relationship between $f_T$, $f_{max}$, $g_m$, $C_{gs}$+$C_{gd}$, input and output resistances ($R_g$+$R_{ch}$ and $R_{ds}$) of FET device [8],

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

$$f_{max} = \frac{f_T}{2} \sqrt{\frac{R_{ds}}{R_g + R_{ch}}}$$

relatively flat $g_m$ and $C_{gs}$+$C_{gd}$ profiles will result in flat $f_T$ and $f_{max}$ features, as shown in the previous figures.
Fig. 2.4.6 Bias-dependent (a) $C_{gs}$ and (b) $C_{gd}$ extracted from on-wafer S-parameter measurements ($f = 2$ GHz) for $1 \mu m \times 100 \mu m$ CC-HEMT device (structure B).

Fig. 2.4.7 The sum of extracted bias-dependent $C_{gs}$ and $C_{gd}$ (frequency = 2 GHz) for $1 \mu m \times 100 \mu m$ CC-HEMT device (structure B).

Fig. 2.4.8 Extraction of the effective channel transit delay from the measured S-parameters for $1 \mu m \times 100 \mu m$ CC-HEMT device (structure B).
Electron transport properties of the minor channel in the CC-HEMT can be evaluated through the bias dependent $f_T$ near pinch-off voltage. Following the method of Moll et al. [43], the channel transit time delay (or the effective electron drift velocity) of the lower channel can be extracted by plotting the total transistor delay ($\tau = \frac{1}{2\pi f_T}$) against the inverse of drain current ($1/I_D$), as shown in Fig. 2.4.13.

A channel transit time delay of 8.8 ps was obtained on the CC-HEMT structure B, which indicates a good channel transport characteristic.

### 2.4.3 Power Performance and Linearity Characteristics

Large-signal load pull measurement was conducted on $1 \, \mu m \times 100 \, \mu m$ devices at 2GHz via a Maury load-pull system on all the three CC-HEMT structures. The results are plotted in Fig. 2.4.14.
Fig. 2.4.9 Power sweep measurement by a load-pull system at 2 GHz on 1 μm x 100 μm devices on the three CC-HEMT structures, with a drain supply voltage of 25 V and a gate bias of -3.5 V.

By tuning the input and output impedance for maximum output power, a linear gain of 16 dB, 22 dB, 16.6 dB together with a power density of 2.3 W/mm, 3.4 W/mm, 1.5 W/mm and a PAE of 29%, 43%, 27% were obtained with a 25 V drain supply voltage for the structure A, B and C, respectively. The substrate was not thinned down and no cooling treatment was employed in the measurement.

Pulse mode I-V characteristics of the devices on the three CC-HEMT structures were also measured by a Diva D265 dynamic I-V analyzer. The results are shown in Fig. 2.4.15.
Fig. 2.4.10 Pulse (circles) mode I-V characteristics of the CC-HEMT structures, with a DC bias of $V_{DS} = 25$ V and $V_{GS} = -3.5$ V.

With a drain bias of 25V, gate bias of -3.5 V (same as the bias condition for power measurement) and a pulse width of 0.5 $\mu$s, all the three structures showed good dynamic I-V characteristics. There was no severe current collapse on these structures. Compare the three curves, it can be found that the three structures have different DC-to-pulse dispersions, structure B exhibited the smallest dispersion, which resulted in the difference of the power performance among these three structures. The reason for the different dynamic I-V characteristics maybe come from the different screening effect of the minor channel on the buffer. Structure B has the strongest screening effect, which can help to reduce the current collapse caused by the virtual gate from the buffer [44] most.
Fig. 2.4.11 IM3 results of the CC-HEMT structures with a fundamental frequency of 2 GHz and an offset of 1 MHz: (a) 3-nm AlGaN; (b) 6-nm AlGaN; (c) 9-nm AlGaN.

To characterize the linearity of the CC-HEMT more directly, two-tone third order intermodulation (IM3) was measured at 2 GHz with an offset frequency of 1 MHz on the three structures. The results are plotted in Fig. 2.4.16. For a 1 μm × 100 μm device, OIP3 of 31.1 dBm, 33.2 dBm and 32.2 dBm were obtained on structure A, B and C, respectively. These values are about 4-5 dBm higher than the value got on our conventional HEMT devices.

As mentioned above, one promising application for AlGaN/GaN HEMTs is the power amplifier in the next generation wireless communication system, such as WCDMA/UMTS, which has stringent requirement of the linearity performance. To characterized the linearity characteristics of the CC-HEMT in a more applicable way,
adjacent channel power ratio (ACPR) measurements were conducted on the CC-HEMT with a 6-nm-thick Al_{0.05}Ga_{0.95}N layer (structure B). The input signal is a modulated signal based on 3GPP WCDMA specifications, with the details listed in table 2-3.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>W-CDMA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uplink</td>
<td>1920-1980 MHz</td>
</tr>
<tr>
<td>Downlink</td>
<td>2110-2170 MHz</td>
</tr>
<tr>
<td>Access method</td>
<td>DS-CDMA</td>
</tr>
<tr>
<td>Duplex procedure</td>
<td>FDD</td>
</tr>
<tr>
<td>Modulation</td>
<td>QPSK</td>
</tr>
<tr>
<td>Pulse shaping</td>
<td>Root-raised cos, α = 0.22</td>
</tr>
<tr>
<td>Chip rate</td>
<td>3.84 Mcp/s</td>
</tr>
<tr>
<td>User data rate</td>
<td>384 kb/s; 2 Mb/s</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>3.84 MHz</td>
</tr>
<tr>
<td>Spacing</td>
<td>5 MHz</td>
</tr>
<tr>
<td>Max. output power</td>
<td>21 dBm (Class IV)</td>
</tr>
</tbody>
</table>

The measuring results of ACPR are shown in Fig. 2.4.17. Both the adjacent (ACPR) and alternative (AltCPR) channel power ratios were measured. Compared with conventional AlGaN/GaN HEMT, at a backoff power of 7 dBm, there are a 5 dBc improvement of ACPR and a 12 dBc improvement in AltCPR in the CC-HEMT, respectively. This indicates an improved linearity performance obtained in the CC-HEMT devices.
Fig. 2.4.12 ACPR and AltCPR versus backoff power in conventional and CC-HEMT.

One thing should be noted here, in the measurement, the actual output power of our CC-HEMT is higher than the conventional one. If we plot the ACPR and AltCPR versus output power, as shown in Fig. 2.4.18, we can find at the same output power, CC-HEMT exhibits a much more improvement over the conventional one. For example, at a output power of 15 dBm, an improvement of about 20 dBc in ACPR and AltCPR was found in CC-HEMT.

Fig. 2.4.13 ACPR and AltCPR versus output power in conventional and CC-HEMT.
2.5 Summary

In this chapter, the design, fabrication, and characterization of Al$_{0.3}$Ga$_{0.7}$N/Al$_{0.05}$Ga$_{0.95}$N/GaN CC-HEMTs were introduced in detail. By employing an Al$_{0.05}$Ga$_{0.95}$N layer as the channel layer instead of the GaN in the conventional AlGaN/GaN HEMTs, the CC-HEMTs exhibit much better $G_m$ linearity at high current levels. From the calculation results of the distribution of the transverse E-field (E$_T$) at the hetero-interface where the 2DEG channel locates, the CC-HEMT structure has a lower E$_T$ than the conventional AlGaN/GaN HEMT structure. The suppressed E$_T$ in the CC-HEMTs can reduce the carrier scattering associated with it and then improve the $G_m$ flatness over a large bias range, which was observed from the DC characteristics of the devices. Furthermore, from the two-tone RF large-signal and ACPR measurements, the CC-HEMTs also exhibited improved linearity performance compared with our conventional AlGaN/GaN HEMTs. This enhanced linearity feature made this kind of new HEMT structure a promising candidate for the applications in high power, high linear amplifiers which are absolutely necessary in the modern wireless communication systems.
CHAPTER 3

ALGAN/GAN/INGAN/GAN DOUBLE HETERO-JUNCTION HEMTS (DH-HEMT) WITH IMPROVED CARRIERE CONFINEMENT

3.1 Channel Engineering for Improved Carrier Confinement in GaN-based HEMTs

As mentioned in Chapter 1, one intrinsic disadvantage of the conventional AlGAN/GaN HEMT structure is the poor carrier confinement in the 2DEG channel. Without a sharp potential barrier at the back side of the 2DEG channel, the conventional AlGAN/GaN HEMTs have a poor carrier confinement which impacts the buffer isolation due to the spill over of carriers from 2DEG channel to buffer. Intensive investigations have been carried out to pursue better buffer isolation in AlGAN/GaN HEMTs. Heikman et al. [45] demonstrated a Fe-doped MOCVD-grown GaN buffer with semi-insulating characteristics. Although better insulation can be obtained on this Fe-doped GaN buffer, the spilling over of the electrons from 2DEG channel to buffer cannot be avoided. By inspecting the band profile of the conventional AlGAN/GaN HEMT structure, one possible way to improve the carrier confinement is to define a 2DEG channel by two sharp potential barriers on both sides of the 2DEG channel, as shown in Fig. 3.1.1(a), the sharp potential barrier at the back side of the 2DEG channel can suppress the spilling over of the carriers to the buffer. To achieve this kind of band profile, the GaN buffer layer in the conventional AlGAN/GaN HEMT structure should be replaced with some other
material which has a higher conduction band than GaN, such as AlGaN. Maeda et al. [46] reported an AlGaN/GaN/AlGaN/GaN double-heterostructure HEMT which exhibited improved carrier confinement. Although this kind of double-heterostructure HEMT can provide an improved carrier confinement, it has some unavoidable drawback. There are two channels which are completely separated by AlGaN layer, which result in two $G_m$ peaks and then degrade the linearity of the device. Micovic et al. [47] demonstrated a double hetero-junction HEMT with improved buffer isolation using AlGaN buffer layer with an Al composition of 4%. Although this structure avoided two 2DEG channels which will affect the devices’ linearity performance, it’s difficult to obtain an AlGaN buffer layer with higher Al composition due to the difficulty of material growth. Besides employing different buffer material to form a sharp potential barrier at the back side of the 2DEG channel, another method is to modify the channel region. One desirable band profile is shown in Fig. 3.1.1(b), where a much sharper potential barrier is formed in the channel layer than the conventional AlGaN/GaN heterostructure.

![Fig. 3.1.1 Two possible band profiles for improved carrier confinement: (a) AlGaN/GaN/AlGaN/GaN double-heterostructure; and (b) AlGaN/InGaN/GaN HEMTs.](image)

59
To achieve this kind of band profile, some material with different crystal properties should be used to replace GaN as the channel layer. A suitable material for this channel layer is InGaN. Simin et al. [48], [49] reported AlGaN/InGaN/GaN HEMTs and MOSHFETs with a thin InGaN layer serving as the channel layer. The biggest obstacle for this approach has been the difficulties in growing single crystal InGaN and obtaining high 2DEG mobility in the InGaN channel. As reported [48], [49], the 2DEG mobility in this InGaN-channel HEMT structure was 730 cm²/Vs, which was lower than the typical value in the conventional AlGaN/GaN HEMT structure (~1000 cm²/Vs).

Although these new structures can fulfill the requirement of better carrier confinement than the conventional AlGaN/GaN HEMT, they induce some other drawbacks. The difficulties in material growth are the major obstacles. High quality AlGaN buffer with high aluminum composition and high quality cluster-free InGaN channel layer are both difficult to grow. The electrical performances of the devices will be severely degraded due to these obstacles.

Although InGaN will degrade the electrical performance of the GaN-based HEMTs when it serves as the channel layer, its unique polarization characteristic makes it a good choice for improving the carrier confinement, as reported in [48], [49]. Compared to AlGaN, InGaN has an opposite polarization field [50], [51]. In the conventional AlGaN/GaN HEMT structure, as shown in Fig. 3.1.2(a), the same polarization filed direction in AlGaN and GaN and the lower conduction band in GaN will result in a potential well for the carriers. While in an InGaN/GaN hetero-
junction, the situation is different. The opposite polarization field in the InGaN layer has an important impact on the band profile of the InGaN/GaN hetero-junction. Although InGaN has a smaller bandgap than GaN, a sharper potential barrier will be formed, as shown in Fig. 3.1.2(b). This special feature makes InGaN a promising candidate for modifying the band profile in the AlGaN/GaN HEMT system, especially when a potential barrier is desired for the improved barrier confinement.

![Figure 3.1.2](image)

Fig. 3.1.2 Schematic band profiles of (a) AlGaN/GaN and (b) InGaN/GaN heterojunctions.

To fulfill the requirement of forming a sharp potential barrier at the back side of the 2DEG channel in AlGaN/GaN-based HEMT structure and avoid the degradation of carrier mobility, a thin InGaN layer can be inserted under the channel to rise up the conduction band. That is, an Al$_x$Ga$_{1-x}$N/GaN/In$_y$Ga$_{1-y}$N/GaN double heterojunction HEMT (DH-HEMT) structure [52], [53] will be formed, whose schematic band profile is shown in Fig. 3.1.3. It can be found that in this “InGaN-notch” DH-HEMT structure, there are two 2DEG channels. The major one is located at the
AlGaN/GaN hetero-interface, while the minor one at the GaN/InGaN hetero-interface. The depth of the minor channel is controlled by the indium composition of the InGaN layer, while the barrier height above the Fermi level at the GaN/InGaN hetero-interface can be adjusted by the thickness of the GaN layer. These parameters will affect the coupling between the carriers in two channels. It is preferred the coupling between the two channels are strong enough and no secondary $G_m$ peak is formed, which will cause linearity degradation.

![Schematic conduction band profile of an AlGaN/GaN/InGaN/GaN DH-HEMT structure.](image)

By employing the channel engineering which features an InGaN layer inserted into the channel region under the 2DEG channel of the conventional AlGaN/GaN heterostructure, the carriers can be confined better and then improve the buffer isolation. By this mean, the burden of growing a semi-insulating GaN buffer, which is quite challenging, can be relaxed.
3.2 Design Procedure of the Al$_x$Ga$_{1-x}$N/GaN/In$_y$Ga$_{1-y}$N/GaN DH-HEMTs

To realize an Al$_x$Ga$_{1-x}$N/GaN/In$_y$Ga$_{1-y}$N/GaN DH-HEMT that can improve the carrier confinement and maintain the electrical performance simultaneously, there are several parameters should be designed carefully, including AlGaN barrier, GaN channel, InGaN layer, and GaN buffer. To simplify the whole design procedure, in the preliminary work, the material parameters of the AlGaN barrier layer in the DH-HEMTs were kept same as our conventional HEMTs, which are supposed to be optimized after countless material growth work. Then there are still three key parameters left: the thickness of the GaN channel, the thickness of the InGaN-notch layer, and the indium composition of the InGaN. To reduce complexity further more, one of them should be fixed to a reasonable value. It seems the thickness of the InGaN layer should be fixed first. The thickness of the InGaN layer affects the barrier height at the back side of the 2DEG channel, which determines the carrier confinement. Too thin an InGaN layer cannot provide enough potential barrier height. On the other hand, it is difficult to grow a very thin InGaN layer (e.g. 1 nm), because the typical growth rate of the InGaN is about 10 nm/min. It’s impossible to control the growth condition very well in a short time. So an InGaN layer with enough thickness is needed in this AlGaN/GaN/InGaN/GaN DH-HEMT structure to ensure an enough barrier height and a well-defined GaN/InGaN hetero-interface. However, the InGaN layer cannot be too thick, either. Crystal quality will suffer from a thick InGaN layer. After the careful analysis based on band profile and material growth
conditions, a thickness of 3 nm was chosen for the InGaN-notch layer, which can provide an enough high potential barrier and the material growth is relatively easy to control.

Now the first parameter should be concerned in the structure design is the thickness of the GaN channel layer. As mentioned in the previous section, the thickness of the GaN channel determines the potential barrier height above the Fermi level at the GaN/InGaN hetero-interface, which will affect the coupling between the two channels. If a thick GaN layer is employed, the two channels will be separated far and completely, few carriers in the minor channel can go over the barrier at the GaN/InGaN hetero-interface, which results in little coupling and two peaks in the $G_m$ curve. This is undesirable because it will cause linearity degradation of the devices. On the other hand, two channels will merge together with a too thin GaN channel, and the overall 2DEG mobility will be degraded because a large part of carriers are located in the InGaN layer, which has a lower mobility due to poor crystal quality. To find out a suitable thickness of the GaN layer, the conduction band profiles of the InGaN-notch HEMT structures with different GaN thicknesses were calculated based on Poisson’s equation and Fermi-Dirac statistics and the results are plotted in Fig. 3.2.1, the indium composition of the InGaN-notch layer was fixed to 10%.
Fig. 3.2.1 Calculated conduction band profiles of the AlGaN/GaN/InGaN/GaN DH-HEMT structures with different GaN channel layer thicknesses.

From Fig. 3.2.1 it can be found that with the increase of the GaN channel layer thickness, the portion occupied by the major channel increases. With a GaN channel layer thickness of 6 nm, the conduction band reaches the Fermi level at the GaN/InGaN hetero-interface. It should be an optimum value that ensure the dominant status of the major channel and avoid two completely separated channels simultaneously. So, in our design, the thickness of the GaN channel layer is fixed to be 6 nm.

The next important parameter in the design of the AlGaN/GaN/InGaN/GaN DH-HEMT structure is the indium composition of the InGaN-notch layer, which directly determines the height of the potential barrier at the back side of the 2DEG channel. The indium composition directly determines the polarization field in the InGaN layer and the conduction band offset at the GaN/InGaN hetero-interface. Higher indium
composition results in more polarization charge and larger conduction band offset at the GaN/InGaN hetero-interface. Although a large potential barrier height is preferred, the large conduction band offset will cause the accumulation of more carriers in the minor channel, which is undesirable. At the same time, as mentioned previously, it's difficult to grow a high quality InGaN layer with high indium composition. To make a comparison, in this work, two DH-HEMT structures which different indium compositions were designed for the device fabrication, one with an In$_{0.05}$Ga$_{0.95}$N notch layer and the other with an In$_{0.1}$Ga$_{0.9}$N notch layer.

Before the material growth, band profiles of these two DH-HEMT structures were also calculated by solving the Poisson's equation and Fermi-Dirac statistics. The results are shown in Fig. 3.2.2, together with the one of our conventional AlGaN/GaN HEMT structure for comparison. The conduction-band offset at InGaN/GaN hetero-interface and the polarization charge density in the InGaN layer are set to be $\Delta E_C = 0.06$ eV, 0.12 eV and $n_p = 3.39 \times 10^{12}$ e/cm$^2$, 6.68$\times$10$^{12}$ e/cm$^2$ for the 10% and 5% indium composition, respectively [50]. The DH-HEMT with 10% indium shows a potential barrier height (measured from the Fermi level) of 400 meV compared to 200 meV in the DH-HEMT with 5% indium. The conduction band minimum of the In$_{0.05}$Ga$_{0.95}$N is also higher than in the In$_{0.1}$Ga$_{0.9}$N, indicating a difference in the threshold voltage between the two structures. This difference was observed in the devices we fabricated, which will be discussed in the latter section.
Fig. 3.2.2 (a) Calculated conduction band profiles of the DH-HEMTs with different indium composition (5% and 10%) and the conventional AlGaN/GaN HEMTs; (b) a close-up of the InGaN layer.

3.3 Material Growth and Device Fabrication

3.3.1 Al0.3Ga0.7N/GaN/In0.3Ga0.7N/GaN DH-HEMTs Growth

The InGaN-notch DH-HEMT structures, with the schematic cross section shown in Fig. 3.3.1, were grown on c-plane sapphire substrates in an Aixtron AIX 2000 HT MOCVD system. After initial desorption at 1200 °C, a GaN nucleation layer was grown at 550 °C, followed by a 2.5-μm-thick unintentionally doped GaN buffer layer. Then the InGaN-notch layer, which is 3-nm thick with low indium composition (5% and 10%), was grown with pure nitrogen carrier gas at 810 °C. Ammonia (NH₃), trimethyl-gallium (TMG) and trimethyl-indium (TMI) were used as source materials. It was followed by the 6-nm-thick GaN channel layer, also grown at 810 °C. The barrier layer was grown at 1100 °C, which consists of a 3-nm undoped spacer, a 15-
nm doped ($2 \times 10^{18}$ cm$^{-3}$) carrier supplier layer, and a 2-nm undoped cap layer. The carrier gas used for the GaN and AlGaN layers is hydrogen.

Fig. 3.3.1 Schematic cross-sectional diagram of the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{GaN}/\text{In}_{y}\text{Ga}_{1-y}\text{N}/\text{GaN}$ DH-HEMT device.

To confirm the successful growth of the InGaN-notch layer, secondary ion mass spectroscopy (SIMS) analysis was performed on the DH-HEMT wafer with 10% indium and the result is shown in Fig. 3.3.2 (a). It can be found there is an obvious indium peak with a full width at half maximum (FWHM) of 3.2 nm, which indicates that an InGaN-notch layer was successfully grown under the GaN channel and no significant indium diffusion occurred during the subsequent high-temperature growth of the AlGaN barrier. A cross-sectional transmission electron microscopy (TEM) picture of the InGaN-notch DH-HEMT structure with 10% indium composition was also taken. As shown in Fig. 3.3.3 (b), a well-defined GaN/InGaN hetero-interface can be found, providing additional evidence for the successful growth of the InGaN-notch layer.
Fig. 3.3.2 (a) SIMS analysis result of the InGaN-notch DH-HMET (10% In) wafer grown in a MOCVD system. An obvious indium peak with a FWHM of 3.2 nm can be observed; (b) TEM picture of the InGaN-notch DH-HMET (10% In). A well-defined interface between the GaN channel layer and the InGaN-notch layer can be found.

To profile the carrier distribution in the InGaN-notch DH-HEMTs, capacitance-voltage (C-V) measurement was carried out on circular Schottky diodes fabricated on the wafers. The carrier distribution profiles of the two samples were extracted from the C-V measurement results and shown in Fig. 3.3.3 along with the C-V characteristics. From Fig. 3.3.3, the carrier concentration in the AlGaN/GaN/InGaN/GaN DH-HMET is estimated to be about $9.22 \times 10^{12}$ cm$^{-2}$ and $9.84 \times 10^{12}$ cm$^{-2}$ for 5% and 10% indium composition, respectively. It can also be found there is only a single peak and no secondary plateau in the carrier distribution profiles, indicating that the minor channel in the InGaN layer is strongly coupled with the major GaN channel due to the small potential barrier (~200 meV and 400 meV above the Fermi level for 5% and 10% indium composition, respectively) at the GaN/InGaN hetero-interface. Furthermore, since most of the electrons are located in
the GaN channel which has a better crystal quality than the InGaN layer, the problem associated with the lower mobility of the InGaN layer was avoided. Instead, the InGaN layer plays the role of creating a potential barrier at the back of the channel for enhanced carrier confinement.

![Graphs showing C-V characteristics](image)

Fig. 3.3.3 C-V characteristics of the InGaN-notch DH-HEMTs with different indium composition, which is measured at 100 kHz through a Schottky diode fabricated on the wafer: (a) 5% indium; (b) 10% indium.

Hall measurement was performed with hall-bridge pattern fabricated on the AlGaN/GaN/InGaN/GaN DH-HEMT wafers. A 2DEG mobility of about 1230 cm²/Vs (1300 cm²/Vs) and a sheet resistance of 550 Ω/sq (480 Ω/sq) were obtained at room temperature on the sample with 5% (10%) indium. Compared with the works employing InGaN channel layer [48], [49], the 2DEG mobility of the AlGaN/GaN/InGaN/GaN DH-HEMT is much higher (than 730 cm²/Vs). Our baseline conventional AlGaN/GaN HEMT structure exhibits a mobility of ~1100 cm²/Vs and a sheet carrier density of $1.4 \times 10^{13}$ cm⁻².
3.3.2 \( \text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN/In}_x\text{Ga}_{1-y}\text{N}/\text{GaN} \) DH-HEMT Device Fabrication

The grown \( \text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN/In}_x\text{Ga}_{1-y}\text{N}/\text{GaN} \) DH-HEMT epilayers were used to fabricate devices via standard process. Device active regions were defined using 300-nm-thick mesa etching by Cl\(_2\)-based inductively coupled plasma reactive ion etching (ICP-RIE). It is followed by the source/drain ohmic contacts formation by a rapid thermal annealing of e-beam evaporated Ti/Al/Ni/Au multilayer at 850°C for 30 seconds. Using on-wafer transfer length method (TLM) patterns, the ohmic contact resistance was typically measured to be 0.8 ohm-mm. Gate electrodes with 1-\( \mu \)m length were then defined by contact photolithography, Ni/Au e-beam evaporation and lift-off, subsequently. The devices have a source-gate spacing of \( L_{sg} = 1 \, \mu \text{m} \) and a gate-drain spacing of \( L_{gd} = 1 \, \mu \text{m} \). Finally, SiN was deposited on the sample by plasma enhanced chemical vapor deposition (PECVD) for device passivation. More details of the device fabrication can be found in Chapter 2 and Appendix A.

3.4 Device Characteristics

3.4.1 DC Characteristics

The DC transfer characteristics \( I_{DS}-V_{GS} \) and transconductance \( (G_m) \) of the AlGaN/GaN/InGaN/GaN DH-HEMT device are plotted in Fig. 3.4.1(a), together with the curves of the conventional AlGaN/GaN HEMT for comparison. The gate dimension of the devices is 1 \( \mu \text{m} \times 10 \, \mu \text{m} \).
The pinch-off voltage of the InGaN-notch DH-HEMTs with 5% and 10% indium composition is -3.6 V and -3.8 V respectively, which is higher than that of the conventional HEMTs (-4.7 V). The difference of the threshold voltage between the two DH-HEMT structures comes from the different conduction band profiles of them. As shown in Fig. 3.2.2(b), the DH-HEMT with an indium composition of 10% has a deeper minor channel and a higher potential barrier, which will result in a higher carrier density. The maximum drain current of the InGaN-notch DH-HEMT is about 750-800 mA/mm, a little bit lower than the conventional one (~900 mA/mm). It was found that the InGaN-notch DH-HEMTs showed a much smaller off-state leakage current than the conventional one. For the DH-HEMT with a 10% indium composition, the leakage current is about 5 μA/mm at $V_{DS} = 10$ V, significantly lower than that of our conventional HEMT devices (~20 μA/mm). For the 5% indium DH-HEMT, the leakage current is about 10 μA/mm, which is smaller than the conventional HEMT but larger than the 10% indium DH-HEMT. This reduced leakage current strongly indicates that the potential barrier provided by the inserted InGaN layer below the 2DEG channel can effectively improve the buffer isolation and an indium composition of 10% is more efficient than 5% in improving the carrier confinement. The peak transconductance of the InGaN-notch DH-HEMT is about 225 mS/mm (for 10% indium) and 200 mS/mm (for 5% indium), which is 10% higher and 4% lower than that in our conventional HEMT devices (~ 205 mS/mm).
Fig. 3.4.1 DC characteristics of the InGaN-notch DH-HEMTs, compared with the conventional one: (a) $I_{DS}-V_{GS}$ and $G_{m}-V_{GS}$ curves with a drain bias of 10 V, about one order of magnitude lower leakage current is obtained on the InGaN-notch DH-HEMTs; (b) $I_{GD}-V_{GD}$ curves, the InGaN-notch ones also exhibit lower gate leakage current.

I-V characteristics of the gate-to-drain Schottky diode were also investigated. The results are plotted in Fig. 3.4.1(b). It is found that, compared with the conventional AlGaN/GaN HEMT, the InGaN-notch DH-HEMT devices also exhibited a lower revise gate leakage current, which is about one order of magnitude lower than the conventional one. One possible reason of this reduced gate leakage current is the cooperation of the indium in the material growth. AFM pictures showed that the InGaN-notch DH-HEMTs exhibited a lower defect density and better surface morphology than the conventional one, as shown in Fig. 3.4.2. Better surface morphology improved the Schottky contact quality, resulted in higher Schottky barrier height and reduced gate leakage current. The DH-HEMTs with 5% and 10% indium composition have similar surface morphology, both can effectively improve the gate isolation.
3.4.2 Small-signal RF Characteristics

Bias-dependent small-signal S-parameters measurements were conducted on 1 μm × 100 μm InGaN-notch DH-HEMT (5% and 10% indium composition) devices, using a HP 4142B modular DC source/monitor and an Agilent 8722ES network analyzer with Cascade microwave probes. The current gain ($|h_{21}|^2$) and the maximum available/stable power gain (MAG/MSG) were extracted from the measured S-parameters and plotted in Fig. 3.4.3(a). The gate bias voltage was -1.5 V and the drain bias voltage was 10 V for both devices. The DH-HEMT device with 5% (10%) indium exhibited a current gain cutoff frequency ($f_T$) of 11.1 GHz (14.5 GHz) and a power gain cutoff frequency ($f_{max}$) of 41.6 GHz (45.4 GHz). Fig. 3.4.3(b) shows the $f_T$ and $f_{max}$ versus drain current curves of the D-mode and E-mode devices, with a drain bias voltage of 10V.
Fig. 3.4.3 RF small signal characteristics of 1 \( \mu m \times 100 \mu m \) InGaN-notch H-HEMT devices with 5\% and 10\% indium composition: (a) frequency-dependent \( |h_{21}|^2 \) and MAG/MSG curves extracted from the measured S-parameters, the bias point is chosen to maximize the cutoff frequencies; (b) bias-dependent \( f_T \) and \( f_{\text{max}} \) curves with a \( V_{DS} \) fixed at 10 V.

Compared with our conventional AlGaN/GaN HEMT devices, the DH-HEMT devices have a similar \( f_T \) but a higher \( f_{\text{max}} \) value. This can be attributed to the lower buffer leakage in the DH-HEMT devices than the conventional ones. Lower buffer leakage will result in larger output resistance of the devices. In the first order approximation, \( f_{\text{max}} \) is related to \( f_T \) in the following equation [8]:

\[
f_{\text{max}} = f_T \cdot \frac{R_{DS}}{2 \sqrt{R_G + R_i}},
\]

where \( R_{DS}, R_G \) and \( R_{CH} \) are the output resistance, gate parasitic resistance and charging resistance of the device, respectively. With larger \( R_{DS} \), the DH-HEMT devices will have a higher \( f_{\text{max}} \) than the conventional ones.

The output resistance of the InGaN-notch DH-HEMT devices and our conventional HEMT device were extracted from the measured S-parameters and the results are plotted together in Fig. 3.4.4.
Fig. 3.4.4 Bias-dependent output resistance ($R_{DS}$) curves extracted from on-wafer S-parameter measurements ($f = 2$ GHz) for 1 $\mu$m $\times$ 100 $\mu$m InGaN-notch DH-HEMT and conventional HEMT devices.

It can be found the InGaN-notch DH-HEMT devices have a larger $R_{DS}$ than the conventional one. Furthermore, the DH-HEMT with 10% indium composition has a larger $R_{DS}$ than 5% indium, which indicates the former one has a better carrier confinement.

In the DH-HEMTs, it is supposed that most carriers are located in the major channel in GaN, which has a better electron transport property than InGaN. To characterize the channel transport properties of the InGaN-notch DH-HEMT, the bias-dependent transistor delay time where extracted from the cutoff frequency by the approximation: $\tau \approx \frac{1}{2\pi f_T}$, and the results are plotted in Fig. 3.4.5. By extrapolating the linear part of the curve to the infinite drain current, the channel transit delay time can be obtained from the interception with the time axis.
Fig. 3.4.5 Channel transient characteristics of the InGaN-Notch HEMT: (a) 5%-indium, only one delay time; (b) 10%-indium, two different delay times can be observed.

For the DH-HEMT with an indium composition of 10%, as shown in Fig. 3.4.5 (b), there are two linear parts with different slopes, which result in a channel delay time of 8.9 ps and 9.9 ps. The smaller delay time is located in the higher current region, corresponding to the major channel in the GaN layer, which has a higher 2DEG mobility. While the larger delay time corresponds to the minor channel in InGaN layer. Although a well-defined hetero-interface can be found between GaN/InGaN in the TEM picture, as shown in Fig. 3.2.2(b), the crystal quality of the InGaN layer was not good enough and mobility degradation was still a big problem, which resulted in a larger channel transit delay time. On the other hand, the DH-HEMT with 5% indium composition exhibited only one delay time, as shown in Fig. 3.4.5(a). This is due to the smaller depth of the minor channel, two channels were completely merged together, which results in an uniform 2DEG mobility.
3.4.3 Large signal RF Characteristics: Power and Linearity

Large-signal RF power measurements were conducted on the InGaN-notch DH-HEMT devices at 2GHz via a Maury load-pull system. By tuning the input and output impedance for maximum output power, a linear gain of 24 dB (25.5 dB) together with an output power density of 1.8 W/mm (3.4 W/mm) and a PAE of 38% (44%) were obtained with a 35 V drain supply voltage on a 1 μm x 100 μm InGaN-notch DH-HEMT device with 5% (10%) indium composition, as shown in Fig. 3.4.6. The substrate was not thinned down and no cooling treatment was employed in the measurement.

![Graphs showing power performances](image)

Fig. 3.4.6 Power performances of the 1 μm x 100 μm DH-HEMT devices with different indium compositions: (a) 5% indium; (b) 10% indium. The gate bias is -2.5 V and the drain bias is 35 V.

To characterize the linearity of the DH-HEMT devices, two-tone third order intermodulation (IM3) was measured at 2 GHz with an offset frequency of 1 MHz. The results are plotted in Fig. 3.4.6. An OIP3 of 28.4 dBm and 29.2 dBm were obtained on 1 μm x 100 μm DH-HEMT devices with 5% and 10% indium composition, respectively.
Fig. 3.4.7 Three-order inter-modulation (IM3) measurement results of 1 μm × 100 μm DH-HEMT with different indium compositions: (a) 5% indium; (b) 10% indium.

3.5 Summary

To pursue better carrier confinement that can improve the buffer isolation in the AlGaN/GaN-based HEMT system, an Al_{0.3}Ga_{0.7}N/GaN/In_{x}Ga_{1-x}N/GaN double hetero-junction HEMT (DH-HEMT) structure was proposed. The design, fabrication, and characterization of the DH-HEMT were introduced in detail. In the conventional AlGaN/GaN HEMT structure, the lack of a sharp potential barrier at the back side of the 2DEG channel results in the poor carrier confinement and then causes large buffer leakage. By employing the unique polarization feature of the InGaN, a thin In_{x}Ga_{1-x}N layer was inserted to the channel region of the conventional AlGaN/GaN HEMT to modify the band profile. A sharp potential barrier was formed at the back side of the 2DEG channel and then improved the carrier confinement. Better buffer isolation was achieved due to this desirable band profile. Compared with the AlGaN/InGaN/GaN HEMT structure which employs InGaN as the channel layer, the DH-HEMT structure avoids the mobility degradation caused by the poor crystal
quality of the InGaN layer by remain the major channel in GaN and make InGaN just to provide a sharp potential barrier at the back side of the 2DEG channel. One order of magnitude smaller buffer leakage current was obtained on an InGaN-notch DH-HEMT with 10% indium composition compared to our conventional AlGaN/GaN HEMTs. Meanwhile, smaller gate leakage current was also obtained on the InGaN-notch DH-HEMT than the conventional one due to the better surface morphology which was induced by indium cooperation in the material growth. The reduced buffer leakage can help to increase the output resistance of the HEMT device, which results in a large $f_{\text{max}}$, a desirable feature for the application of high frequency power amplifier.
CHAPTER 4

ENHANCEMENT-MODE HEMTS ON ALGAN/GAN/INGAN/GAN DH-HEMTS WITH STATE-OF-THE-ART PERFORMANCES

4.1 Motivation for the AlGaN/GaN-based Enhancement-mode Devices

Up to now, most works on the AlGaN/GaN HEMTs are focused on the depletion-mode (D-mode) devices [27], [54]-[57]. However, from the application point of view, the enhancement-mode (E-mode) HEMT devices may have many advantages. For the applications such as high frequency power amplifiers (PAs) and low noise amplifiers (LNAs), E-mode devices can simplify the circuit configuration by eliminating the negative power supply, because there is no need to use a negative bias voltage to pich-off the device. Although with smaller maximal forward gate bias, the E-mode devices provide smaller drain current and then lower power density, they can still offer enough power density for high power applications. For example, the reported record of power density on AlGaN/GaN HMETs can be as high as 30 W/mm [27], while the commercial devices only supply a value of about 2 W/mm. On the other hand, with the excellent high temperature stability of the III-nitrides, AlGaN/GaN HEMTs are also promising candidates for the applications in high temperature, high speed digital circuits. The integration of D-mode and E-mode devices in the direct-coupled FET logic (DCFL) can reduce the complexity of the circuit.
Some works have been reported on the E-mode AlGaN/GaN HEMTs. Khan et al. [58] demonstrated an E-mode HEMT by using a thin (10 nm) AlGaN barrier, but the transconductance is only 23 mS/mm, which is much lower than the D-mode HEMTs. Rajan et al. [58] reported an E-mode HEMTs by growing a N-faced AlGaN barrier, some re-growth technology is needed to form the source/drain electrodes on the E-mode epilayer, which makes the process much more complex. Some other works started with D-mode HEMTs. By employing some kinds of processes techniques, such as recessed-gate [59]-[61], special gate metal [62] and selectively grown p-n junction gate [63], the threshold voltage was shifted towards 0 V. Although all of these technologies can realize E-mode GaN-based HEMTs, there are many drawbacks of them and the devices performances will be degraded compared with D-mode HEMTs.

To fabricate high-performance AlGaN/GaN-based E-mode HEMTs with simpler and reliable process, some new technique should be developed. Furthermore, due to the difficulty of growing an E-mode AlGaN/GaN HEMT epilayers, this new technique should use the mature D-mode AlGaN/GaN HEMTs as the start-off point.

### 4.2 E-mode AlGaN/GaN HEMTs Fabrication

As mentioned above, the most desirable way to realize E-mode AlGaN/GaN HEMTs is to use some technology to convert the conventional D-mode AlGaN/GaN HEMTs into E-mode. A simple method should be employed to shift the threshold voltage of the D-mode HEMTs towards zero. By investigating the operation
principle of the AlGaN/GaN HEMTs, when the carrier density in the 2DEG channel goes to zero, the channel will be totally depleted and E-mode HEMTs can be realized. From the view of band profile, to deplete the 2DEG channel, the conduction band profile should be modified by some means. The most efficient way is to induce some negative charges in the barrier layer, which can raise the conduction band and no 2DEG channel can be formed under the Fermi level, as shown in Fig. 4.2.1.

Fig. 4.2.1 Schematic conduction band profiles of (a) conventional D-mode AlGaN/GaN HEMTs, and (b) E-mode AlGaN/GaN HEMTs in which the 2DEG channel is depleted by fixed negative charges in the barrier.

To get more quantitative analysis results of how the fixed negative charges deplete the 2DEG channel, calculations based on the Poisson’s equation and Fermi-Dirac statistics were carried out. The calculations were based on our conventional AlGaN/GaN HEMT structure. The AlGaN barrier consists of a 2-nm-thick cap layer, a 15-nm-thick carrier supply layer (doped at $2\times10^{18}$ cm$^{-3}$), and a 3-nm-thick spacer,
the background carrier concentration is set to be $10^{16}$ cm$^{-3}$ by assumption, which consists with the value extracted from C-V measurements. To demonstrate the effect of the distribution profile of the negative charge on the depletion of 2DEG channel, three different kinds of profiles of the negative charge distribution were applied to the calculations: constant distribution, linear distribution decreases from the surface to the channel, and Gaussian distribution.

![Graphs showing different charge distributions](image)

(a) D-mode (b) Constant Distribution (c) Linear Distribution (d) Gaussian Distribution

Fig. 4.2.2 Calculated conduction band profiles with different fixed negative charge distributions, with the distribution profiles in the insets: (a) conventional D-mode HEMTs; (b) constant distribution; (c) linear distribution; and (d) Gaussian distribution.

By tuning the peak value of the fixed negative charge density, the 2DEG channel in the AlGaN/GaN HEMTs can be completely depleted. The results are shown in Fig.
4.2.2. For a constant distribution, a charge density of $1 \times 10^{19}$ cm$^{-3}$ is needed; for a linear distribution, the charge density decreases from $3 \times 10^{19}$ cm$^{-3}$ to $1 \times 10^{16}$ cm$^{-3}$ is needed; and for the Gaussian distribution, the charge density is $4.5 \times 10^{19}$ cm$^{-3}$ at surface, decreases to $5 \times 10^{16}$ cm$^{-3}$ at the AlGaN/GaN hetero-interface.

From the calculation we can found suitable fixed negative charges in the AlGaN barrier can effectively deplete the 2DEG channel and turn the device into depletion-mode. Then how to induce the required fixed negative charges into the AlGaN barrier? Recently we developed a fluoride-based plasma treatment technique [58] to fulfill the target. The basic principle is shown in Fig. 4.2.3.

![Diagram](image)

Fig. 4.2.3 Principle of CF$_4$ plasma treatment on conventional AlGaN/GaN D-mode HEMTs, where the fixed F$^-$ in AlGaN barrier can deplete the 2DEG channel.

After the definition of gate window by photolithography, by applying a CF$_4$ plasma on the conventional AlGaN/GaN HEMTs, negatively charged fluorine ions can be induced into the AlGaN barrier and kept there stably. By tuning the treatment
conditions (power, time, etc.), these fixed fluorine ions can modulate the conduction
band profile and then exactly deplete the 2DEG channel, as described in Fig. 4.2.3.

4.3 Material Preparation and Device Fabrication

To demonstrate the state-of-the-art performance of E-mode GaN-based HEMTs,
the newly developed Al$_{0.3}$Ga$_{0.7}$N/GaN/In$_{0.1}$Ga$_{0.9}$N/GaN DH-HEMT epilayers were
used for the fabrication devices. For the details of the material growth, please refer to
Chapter 3. As discussed in Chapter 3, the DH-HEMT has an improved carrier
confinement and lower buffer leakage, which can help to improve the overall
performance of the devices.

To make a comparison, both D-mode and E-mode devices were fabricated on the
same DH-HEMT structure. Device active regions were defined using 300-nm-thick
mesa etching by Cl$_2$-based ICP-RIE. It is followed by the source/drain ohmic
contacts formation by a rapid thermal annealing of e-beam evaporated Ti/Al/Ni/Au
multilayer at 850°C for 30 seconds. Using on-wafer TLM patterns, the ohmic contact
resistance was typically measured to be 0.8 ohm-mm. The gates of the D-mode and
E-mode HEMTs were processed in two separate steps. First, gate electrodes of the D-
mode HEMTs with 1-μm length were then defined by contact photolithography,
Ni/Au e-beam evaporation and lift-off, subsequently. The devices have a source-gate
spacing of $L_{sg} = 1$ μm and a gate-drain spacing of $L_{gd} = 1$ μm. The gate electrodes of
the E-mode devices were then defined by photolithography. Before the deposition of
the gate metal, the sample was treated by CF$_4$ plasma in an RIE system at an RF plasma power of 150 W for 150 s. After Ni/Au e-beam evaporation and lift-off, a post-gate rapid thermal annealing (RTA) was conducted at 400 °C for 10 minutes. Finally, SiN was deposited on the sample by PECVD for device passivation. Details of the device fabrication can be found in Chapter 2 and Appendix A.

4.4 Device Characteristics

4.4.1 DC Characteristics

DC measurements were performed on the fabricated D-mode and E-mode DH-HEMT devices with a gate dimension of 1 μm × 10 μm. The DC output characteristics $I_{DS}$-$V_{DS}$ and transfer characteristics $I_{DS}$-$V_{GS}$ are plotted in Fig. 4.4.1. In Fig. 4.4.1(b), by extrapolating the linear part of the transfer curve to zero current, the threshold voltage of the E-mode device is estimated to be around 0 V, which was shifted by 3.8 V from the D-mode device. Compared with D-mode device, the maximum gate bias that can be applied on the E-mode device is higher, which is about +3 V here (for D-mode one, the maximum gate bias is around +1 V). The improvement of the maximum gate bias is due to modified band profile of the plasma-treated sample. As shown in Fig. 4.2.2, after inducing the negative charges into the AlGaN barrier, the barrier height in the AlGaN layer was increased compared with the conventional D-mode structure. This higher barrier can help to increase the forward turn-on voltage of the Schottky contact form on the wafer and
then a higher maximum gate bias voltage can be applied on the devices, which is a
desirable feature. With a gate bias of +3 V, a maximum drain current density of
about 500 mA/mm was obtained on the E-mode DH-HEMTs, which is about 66% of
the value on D-mode ones. This reduction is due to the limited gate bias swing that
can be applied on the E-mode device. For D-mode one, the gate bias swing is about 5
V, while for the E-mode one the gate bias swing is about 3 V. The peak
transconductance of the E-mode DH-HEMTs is ~205 mS/mm, which is about 9%
lower than the D-mode DH-HEMTs and comparable to the conventional
AlGaN/GaN HEMTs. These results indicate that the CF4 plasma treatment followed
by annealing can effectively shift the threshold voltage of the D-mode HEMTs
towards zero and no obvious degradation in DC characteristics will be introduced.

![Graphs](image)

**Fig. 4.4.1** DC characteristics of the D-mode and E-mode DH-HEMTs: (a) $I_{DS}$-$V_{DS}$
curves, for D-mode, $V_{GS}$ starts from +1 V with a step of -1 V, for E-mode, $V_{GS}$ starts
from +2.5 V with a step of -0.5 V; (b) $I_{DS}$, $G_{m}$-$V_{GS}$ curves, the drain bias is 10 V.

From the DC characteristics, it can be found that the E-mode devices can endure
a much higher forward bias (> +3 V) than the D-mode ones (+1V). The improvement
comes from the increase of conduction band in AlGaN barrier, which is induced by
the fixed fluorine ions. The raised potential can improve the gate isolation and increase the turn-on voltage of the gate Schottky contact. Compared to other E-mode HEMTs fabrication technologies, this is an obvious advantage which can ensure higher current capability.

4.4.2 RF Small-signal and Large-signal Characteristics

Bias-dependent small-signal S-parameters measurements were conducted on 1 \( \mu \text{m} \times 100 \ \mu \text{m} \) D-mode and E-mode DH-HEMT (with 10% indium composition) devices, using a HP 4142B modular DC source/monitor and an Agilent 8722ES network analyzer with Cascade microwave probes. The current gain \( (|h_{21}|^2) \) and the maximum available/stable power gain (MAG/MSG) were extracted and plotted in Fig. 4.4.2(a). The gate bias voltage was -1.5 V for the D-mode device and 1 V for the E-mode device, respectively. The drain bias voltages applied on these two kinds of devices are both 10 V. The D-mode (E-mode) DH-HEMT devices exhibited similar RF small signal characteristics. A cutoff frequency of current gain \( (f_t) \) of 14.5 GHz (14.9 GHz) and a cutoff frequency of power gain \( (f_{\max}) \) of 45.4 GHz (46.2 GHz) were obtained. Fig. 4.42(b) shows the \( f_t \) and \( f_{\max} \) versus drain current curves of the D-mode and E-mode devices, with a drain bias voltage of 10 V.
Fig. 4.4.2 RF small signal characteristics of 1 μm × 100 μm D-mode and E-mode DH-HEMT devices: (a) frequency-dependent $|h_{21}|^2$ and MAG/MSG curves extracted from the measured S-parameters, the bias point is chosen to maximize the cutoff frequencies; (b) bias-dependent $f_T$ and $f_{max}$ curves with $V_{DS}$ fixed at 10 V.

Large-signal RF power measurements were also conducted on D-mode and E-mode DH-HEMT devices at 2GHz with a Maury load-pull system. By tuning the input and output impedance for maximum output power, a linear gain of 26 dB together with a power density of 3.1 W/mm and a PAE of 49 % were obtained with a gate bias voltage of 0.5 V and a 35 V drain supply voltage on a 1 μm × 100 μm E-mode device, as shown in Fig. 4.4.3(a). The results of the D-mode device with same dimension are provided in Fig. 4.4.3(b) for comparison. The substrate was not thinned down and no cooling treatment was employed in the measurement. It was found that the E-mode DH-HEMT exhibited comparable power performance as its D-mode counterpart fabricated on the same wafer. To our best knowledge, this is the first power performance reported on the E-mode GaN-based HEMT devices.
Fig. 4.4.3 Power performances of 1 μm × 100 μm (a) E-mode and (b) D-mode DH-HEMT devices measured at 2 GHz with a drain supply voltage of 35 V. For E-mode one, $G_{\text{Linear}} = 26$ dB, $P_{\text{max}} = 3.12$ W/mm, PAE = 49%; for D-mode one, $G_{\text{Linear}} = 25.5$ dB, $P_{\text{max}} = 3.46$ W/mm, PAE = 44%.

Fig. 4.4.4 Two-tone measurement result of a 1 μm × 100 μm E-mode DH-HEMT device, with an OIP3 of 34.7 dBm.

To characterize the linearity of the E-mode DH-HEMT devices, two-tone third order intermodulation (IM3) was measured at 2 GHz with an offset frequency of 1 MHz. The result is plotted in Fig. 4.4.4. An OIP3 of 34.7 dBm was obtained on a 1 μm × 100 μm E-mode DH-HEMT device, which is about 5.5 dBm higher than its D-mode counterpart. The improvement in the linearity can be ascribed to the smaller maximum gate bias applied on the E-mode DH-HEMTs than the D-mode ones, which induces lower transverse E-field at the Al$_{0.3}$Ga$_{0.7}$N/GaN hetero-interface.
4.4.3 Noise Characteristics

By following the noise characterization which was done in [D3] and [D11], on-wafer high-frequency noise performances of the D-mode and E-mode DH-HEMT devices were measured using Maury Microwave’s MT982B01 load-pull system with Agilent N8975A Noise Figure Analyzer. Fig. 4.4.5 shows the minimum noise figure $N_{\text{min}}$ and the associated gain of D-mode and E-mode DH-HEMT devices with 1-µm gate length at 2 GHz with different drain currents. The gate-to-drain and gate-to-source spaces of the devices are both 1 µm. For D-mode (E-mode) devices, a $N_{\text{F, min}}$ of 0.79 dB (0.63 dB) was obtained with a drain current density of 150 mA/mm (100 mA/mm) (about 20% (21%) of the maximum drain saturation current) and drain bias voltage of 5 V (3 V). Compare the bias-dependent noise performance of the D-mode and E-mode DH-HEMTs, it is found that in the low bias current region, the E-mode one has a smaller $N_{\text{F, min}}$ value than the D-mode one, which is desired in the LNA design.

Fig. 4.4.5 Bias-dependent minimum noise figure and associated gain of a 1 µm (a) D-mode (b) E-mode DH-HEMTs.
The smaller $\text{NF}_{\text{min}}$ at low current levels in the E-mode device comes from the lower gate leakage current in the E-mode device than the D-mode one. As shown in Fig. 4.4.6(a), in the low current region, the E-mode DH-HEMTs showed a much lower gate leakage current than the D-mode one, which resulted in the lower noise figure which is determined by [64]:

$$F_{\text{min}} = 1 + \frac{R_{\text{in}}}{R_{\text{opt}}} + b\frac{R_{\text{opt}}^2 + X_{\text{opt}}^2}{R_{\text{opt}}} + \frac{a}{R_{\text{opt}}} \left| R_{\text{in}} + R_{\text{opt}} + j\left(X_{\text{opt}} + \frac{1}{\omega C_{\text{gr}}} \right) \right|^2,$$

where

$$a = g_m \Gamma \left( \frac{\omega}{\alpha_r} \right)^2, \quad b = \frac{qI_{\text{gs}}}{2kT}, \quad \omega_r = \frac{g_m}{C_{\text{gr}}}, \quad R_{\text{in}} = R_g + R_s + R_l.$$

The lower gate leakage current in the E-mode DH-HEMTs was caused by the modulated barrier height in AlGaN barrier in it. As shown in Fig. 4.4.6(b), the barrier was raised up by the fixed negative charges in the AlGaN barrier after plasma treatment, which resulted in better Schottky contacts and lower gate leakage current.

![](image1.png)

Fig. 4.4.6 (a) Gate leakage current of D-mode and E-mode DH-HEMTs; (b) Conduction band profile of E-mode DH-HEMTs.

Driven by the optimized bias condition, frequency-dependent noise performances of this D-mode and E-mode DH-HEMT device were measured over the frequency
range from 1 GHz to 12 GHz. The results are plotted in Fig. 4.4.7. For the frequency of 1 GHz, the \(N_{F_{\text{min}}}\) of the device is higher than that at 2 GHz, this maybe comes from the system error. For this 1 \(\mu\)m-gate length D-mode (E-mode) DH-HEMT device, a \(N_{F_{\text{min}}}\) of 0.8 dB (0.62 dB) and an associated gain \((G_a)\) of 19.8 dB (18.3 dB) were obtained at 2 GHz, a \(N_{F_{\text{min}}}\) of 5.6 dB (5.1 dB) and \(G_a\) of 8.3 dB (5.7 dB) were obtained at 12 GHz.

![Diagrams](image)

Fig. 4.4.7 Frequency-dependent noise characteristics of the D-mode and E-mode DH-HEMTs with a gate length of 1\(\mu\)m: (a) \(N_{F_{\text{min}}}\); (b) \(\Gamma\); (c) \(r_o\); and (d) \(G_a\).
To the best knowledge of us, it is also the first time that the noise characteristics of E-mode GaN-based HEMTs are analyzed. In parallel comparison with D-mode HEMTs, there was no degradation in the noise performance in E-mode HEMTs.

4.5 Summary

In this chapter, the recently developed technique for fabricating E-mode HEMTs using fluoride-bade plasma treatment followed with annealing was introduced. To demonstrate the state-of-the-art performances of GaN-based E-mode HEMTs, this technology was employed on our newly-developed InGaN-notch DH-HEMT structures which can provide improved carrier and lower buffer leakage current. E-mode HEMTs with a threshold voltage near 0 V was successfully fabricated on our Al$_{0.3}$Ga$_{0.7}$N/GaN/In$_{0.1}$Ga$_{0.9}$N/GaN DH-HEMT structure. DC, RF small- and large-signal, and noise characteristics were studied on the E-mode DH-HEMTs and no performance degradation was found compared with its D-mode counterparts.

Compared with other techniques, the fluoride-base plasma treatment has many advantages in the fabrication of E-mode HEMTs. For example, higher current density, better reliability and uniformity, self-align gate, and simpler process. These features make it a promising new technology for the GaN-base micro-processing.
CHAPTER 5

CONCLUSIONS

5.1 Conclusion

In this thesis work, there are three main parts work of the GaN-based HEMT's, namely composite-channel HEMT (CC-HEMT), InGaN-notch double hetero-junction HEMT (DH-HEMT), and the enhancement-mode HEMTs with state-of-the-art performances.

Differs from the most work in the field of GaN-based HEMTs, the work done in this thesis mainly focus on the channel region of the GaN-based HEMTs instead of the barrier or the buffer layers. By modifying the channel region of the AlGaN/GaN-based HEMTs with inserting additional III-nitride alloys, novel HEMT structures with enhanced performances have been proposed and designed aiming improvement in different figure of merits of the device.

Firstly, an $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{Al}_{0.05}\text{Ga}_{0.95}\text{N}/\text{GaN}$ composite-channel HEMT (CC-HEMT) structure was designed by employing a thin $\text{Al}_{0.05}\text{Ga}_{0.95}\text{N}$ layer as the channel layer instead of GaN in the conventional AlGaN/GaN HEMTs. By calculation, it was found the transverse electrical field ($E_T$) at the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{Al}_{0.05}\text{Ga}_{0.95}\text{N}$ hetero-interface was reduced compared with the conventional $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{GaN}$ heterostructure. The scattering at the hetero-interface, which is one possible cause of the reduction of the carriers' saturation velocity in the channel, is then alleviated and
the $G_m$ compression at high current levels was suppressed. A series of CC-HEMT devices with different epilayer parameters were designed, grown, and fabricated. From the DC IV characteristics, two-tone RF large-signal, and ACPR measurements, improved linearity performance in term of $G_m$ flatness over large bias range, OPI3, and ACPR were observed on the CC-HEMT. Enhanced linearity performance of the CC-HEMTs can relax the linearity burden of the power amplifiers used in large signal operations.

Secondly, to improve the carrier confinement in the conventional AlGaN/GaN HEMTs, channel engineering was applied by employing a thin InGaN with low indium composition (10%) to modify the band profile. In the conventional AlGaN/GaN HEMTs, there is not a good potential barrier under the 2DEG channel, which results the spilling over of the carriers from the 2DEG channel to the GaN buffer. Because usually the GaN buffer is not semi-insulating as it is desired, the poor carrier confinement in the conventional AlGaN/GaN will cause buffer isolation problem, the large buffer leakage will reduce the output resistance of the device and then degrade the large-signal power performance of the device. To solve this intrinsic problem associated with the conventional AlGaN/GaN HEMTs, an $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{GaN/In}_{0.1}\text{Ga}_{0.9}\text{N}/\text{GaN}$ double hetero-junction HEMT (DH-HEMT) structure was developed. The inserted InGaN layer can raise the conduction band under the 2DEG channel and form a sharp potential barrier which helps to improve the carrier confinement. Better buffer isolation was then obtained on this DH-HEMT structure with better carrier confinement. From the DC measurements on the DH-
HEMT devices with 10% indium composition, one order of magnitude lower buffer leakage was obtained compared with our conventional AlGaN/GaN HEMTs. Lower gate leakage current was also observed on the DH-HEMTs than the conventional ones, which is believed due to the cooperation of the indium in the material growth. Higher output resistance was obtained on the DH-HEMTs than the conventional ones by extraction from the small-signal S-parameter measurements.

Enhancement-mode (E-mode) GaN-based HEMTs are of great research interest recently because of the elimination of negative power supplier in the circuit. The previous works reported by other groups on the E-mode GaN-bases HEMTs didn't show comparable performances of the E-mode devices as the depletion-mode (D-mode) ones. To demonstrate the state-of-the-art performances of the E-mode GaN-base HEMTs, a recently developed CF₄ plasma treatment technology followed by annealing was used for fabricating E-mode HEMTs on the D-mode InGaN-notch DH-HEMT structures. Fluorine ions were induced into the AlGaN barrier and fixed there stably. These negatively charged ions can deplete the 2DEG channel under the gate electrode and then make E-mode HEMTs possible. E-mode HEMTs were successfully fabricated on the newly designed DH-HEMT structure by employing this new technology. RF power and noise characteristics of E-mode GaN-based HEMTs were reported for the first time. Detailed DC, RF and noise characteristics showed this fluoride-based plasma treatment technology is reliable, effective and simple without performance degradation, which is a promising technology to be employed in the fabrication of E-mode GaN-based HEMTs.
5.2 Suggestions for Future Work

As discussed in Chapter 2, for the CC-HEMT structure which employs an AlGaN channel layer with a constant aluminum composition of 5%, although the $G_m$ linearity was improved compared with the conventional AlGaN/GaN HEMTs, there will be two hetero-interfaces, which may cause two 2DEG channels and affect the linearity performance. To eliminate this undesirable feature, some new CC-HEMT-based structure can be designed and characterized. For example, an AlGaN channel layer with graded aluminum composition increases from GaN at buffer side to $\text{Al}_x\text{Ga}_{1-x}\text{N}$ at barrier side can be used. In such a structure, there is only one 2DEG channel and the problem of linearity degradation caused by two separated 2DEG channels can be avoided. Further improvement of linearity is supposed to be achieved on this kind of new CC-HEMT structure.

Secondly, the plasma treatment technology can be utilized in some other fields. For example, it can be used to treat other region of the device instead of the gate in the case of E-mode HEMTs. Because negative charges can be introduced into the AlGaN barrier and stay there stably, they can be used to modify the electrical field in the AlGaN/GaN-based HETMs, which can affect the breakdown, access resistance, and some other features of the devices.

Finally, some more modeling and extraction work can be done based on the equivalent circuit of the GaN-based HEMTs. It is believed that the access resistance of the GaN-based HEMTs will be affected by the DC bias applied on the gate electrode. Some transfer line method with gate electrode (gated-TLM) can be
designed to extracted this gate-bias-dependent access resistance of the GaN-based HEMTs. On the other hand, some modeling work can be carried out on the noise characteristics of the GaN-base HEMTs.
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[40] J. Liu, Y. G. Zhou, R. M. Chu, Y. Cai, K. J. Chen, and K. M. Lau, "Highly Linear Al$_{0.3}$Ga$_{0.7}$N/Al$_{0.05}$Ga$_{0.95}$N/GaN Composite-Channel HEMTs," *IEEE Electron Device Lett.*, vol. 26, no. 3, pp. 145-147, Mar. 2005.


Conference on Nitride Semiconductors, We-ED2-5, Bremen, Germany, Aug.


APPENDIX A

PROCESS FLOW FOR THE FABRICATION OF GAN HEMTs

1 Mesa Isolation

Solvent Cleaning

(1) Check the resistivity of DI water. It should be > 17 MΩ.
(2) ACE 3 minutes, ultrasonic 1 minute.
(3) ISO 3 minutes, ultrasonic 1 minute.
(4) DI water spray rinse, 4 cycles.
(5) Blow dry with N₂ gun.
(6) Dehydration bake, 120 °C, 10 minutes in oven.

Photoresist Application

(1) Cool down after dehydration, 5 minutes.
(2) Put wafer on spinner chuck with vacuum on, blow with N₂.
(3) Coat AZ 703 photoresist.
(4) Spin at 4000 rpm for 30 seconds, ~1 μm thick.
(5) Soft bake, 90 °C, 1 minute, on hotplate.

Photoresist Exposure and Development

(1) Exposure for 3.8 seconds, Karl Suss MA6 Aligner, low-vacuum contact mode.
(2) Post-exposure bake, 110 °C, 1 minute, on hotplate.
(3) Develop in FHD-5 for 60 seconds.
(4) DI water spray rinse, 4 cycles.
(5) Check under microscopy.

Oxygen Plasma Descum of Photoresist

(1) Chamber pressure = 300 mT of O₂.
(2) Temperature: 70 °C.
(3) Run for 0.7 minute.
ICP Mesa Etch

(1) Cl₂ flow rate = 15.0 sccm.
(2) He flow rate = 10.0 sccm.
(3) Chamber pressure = 5.0 mTorr.
(4) Power = 135 W.
(5) 40 seconds etch, 300 nm.

2 Source/Drain Electrodes Definition

Solvent Cleaning

(1) Check the resistivity of DI water. It should be > 17 MΩ.
(2) ACE 3 minutes, ultrasonic 1 minute.
(3) ISO 3 minutes, ultrasonic 1 minute.
(4) DI water spray rinse, 4 cycles.
(5) Blow dry with N₂ gun.
(6) Dehydration bake, 120 °C, 10 minutes in oven.

Photoresist Application

(1) Cool down after dehydration, 5 minutes.
(2) Put wafer on spinner chuck with vacuum on, blow with N₂.
(3) Coat AZ 703 photoresist.
(4) Spin at 4000 rpm for 30 seconds, ~1 μm thick.
(5) Soft bake, 90 °C, 1 minute, on hotplate.

Photoresist Exposure and Development

(1) Exposure for 3.8 seconds, Karl Suss MA6 Aligner, low-vacuum contact mode.
(2) Post-exposure bake, 110 °C, 1 minute, on hotplate.
(3) Develop in FHD-5 for 60 seconds.
(4) DI water spray rinse, 4 cycles.
(5) Check under microscopy.

Oxygen Plasma Descum of Photoresist

(1) Chamber pressure = 300 mT of O₂.
(2) Temperature: 70 °C.
(3) Run for 0.7 minute.
Surface Preparation

(1) Mix a dilute solution of HCL:H₂O = 1:10.
(2) Dip in dilute HCl for 15 seconds.
(3) DI water spray rinse, 4 cycles.
(4) Blow dry with N₂ gun.

Evaporation

(1) Mount wafer into e-beam chamber.
(2) Pump down to below 10⁻⁶ torr.
(3) Deposit material:

<table>
<thead>
<tr>
<th>Material</th>
<th>Thickness</th>
<th>Deposition Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti</td>
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</tr>
<tr>
<td>Al</td>
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<td>3.0 Å/sec</td>
</tr>
<tr>
<td>Ni</td>
<td>500 Å</td>
<td>2.0 Å/sec</td>
</tr>
<tr>
<td>Au</td>
<td>800 Å</td>
<td>3.0 Å/sec</td>
</tr>
</tbody>
</table>

Liftoff

(1) Soak wafer in ACE until metal becomes loose.
(2) Rinse with ISO.
(3) DI water spray rinse, 4 cycles.
(4) Blow dry with N₂ gun.
(5) Check under microscopy, and then measure the metal thickness.

Annealing

(1) Run the RTA 2~3 times with a dummy wafer to check the temperature stability.
(2) Load wafer into the chamber slowly.
(3) Wait several minutes before heating up, anneal at 850 °C for 30 seconds.
(4) Unload wafer after RTA cools down.
(5) Check Ohmic contacts with I-V measurement.

3 Gate Electrodes Definition

Solvent Cleaning
(1) Check the resistivity of DI water. It should be > 17 MΩ.
(2) ACE 3 minutes, ultrasonic 1 minute.
(3) ISO 3 minutes, ultrasonic 1 minute.
(4) DI water spray rinse, 4 cycles.
(5) Blow dry with N₂ gun.
(6) Dehydration bake, 120 °C, 10 minutes in oven.

Photoresist Application

(1) Cool down after dehydration, 5 minutes.
(2) Put wafer on spinner chuck with vacuum on, blow with N₂.
(3) Coat AZ 703 photoresist.
(4) Spin at 4000 rpm for 30 seconds, ~1 μm thick.
(5) Soft bake, 90 °C, 1 minute, on hotplate.

Photoresist Exposure and Development

(1) Exposure for 3.8 seconds, Karl Suss MA6 Aligner, low-vacuum contact mode.
(2) Post-exposure bake, 110 °C, 1 minute, on hotplate.
(3) Develop in FHD-5 for 60 seconds.
(4) DI water spray rinse, 4 cycles.
(5) Check under microscopy.

Oxygen Plasma Descum of Photoresist

(1) Chamber pressure = 300 mT of O₂.
(2) Temperature: 70 °C.
(3) Run for 0.7 minute.

Surface Preparation

(1) Mix a dilute solution of HCl:H₂O = 1:10.
(2) Dip in dilute HCl for 15 seconds.
(3) DI water spray rinse, 4 cycles.
(4) Blow dry with N₂ gun.

Evaporation

(1) Mount wafer into e-beam chamber.
(2) Pump down to below $10^{-6}$ torr.

(3) Deposit material:

<table>
<thead>
<tr>
<th>Material</th>
<th>Thickness</th>
<th>Deposition Rate</th>
</tr>
</thead>
<tbody>
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<td>Ni</td>
<td>200 Å</td>
<td>2.0 Å/sec</td>
</tr>
<tr>
<td>Au</td>
<td>3000 Å</td>
<td>3.0 Å/sec</td>
</tr>
</tbody>
</table>

Liftoff

(1) Soak wafer in ACE until metal becomes loose.
(2) Rinse with ISO.
(3) DI water spray rinse, 4 cycles.
(4) Blow dry with N$_2$ gun.
(5) Check under microscopy, and then measure the metal thickness.
APPENDIX B

DEVICE CHARACTERIZATION

1. DC Characterization

Generally, the on-wafer statistic and dynamic DC characterization of devices can be performed by using the semiconductor parameter analyzer and the dynamic I-V analyzer (DIVA), respectively.

Fig. B.1(a) shows the configuration of the static DC measurement. It consists of a semiconductor parameter analyzer and an on-wafer probe station (not shown here). Usually a small device with the shape shown in Fig B.1(b) is used for static DC measurements. The gate dimension is 1 μm x 10 μm. The device is connected to the semiconductor parameter analyzer with pin-shape probes and cables.

![Diagram showing configuration of static DC measurement](image)

Fig. B.1 (a) Configuration of the static DC measurement with a semiconductor parameter analyzer; (b) the shape of the device for the static DC measurement.
Usually, the measurements include the output characteristic $I_{DS}-V_{DS}$, the transfer characteristic $I_{DS}-V_{GS}$, the transconductance characteristic $G_{m}-V_{GS}$, the I-V characteristic of the gate-to-drain Schottky diode $I_{GD}-V_{GD}$, and the off-state breakdown voltage $V_{BR}$. These are basic DC performances of the devices and provide quick-check after the fabrication of the devices.

For the dynamic I-V characterization, a dynamic IV analyzer (DIVA) controlled by PC is used together with GSG (ground-signal-ground) probes and the on-wafer probe station. The configuration of the measuring system is shown in Fig. B.2(a). The devices for the dynamic I-V measurements have a larger gate dimension than the ones used in the static DC characterization. The shape of the device and the GSG probe are shown in Fig. B.2(b) and (c), respectively. The gate dimension is $1 \mu m \times 100 \mu m$.

In the dynamic IV measurements, from the PC software, the quiescent bias point, the pulse width and duty cycle, the steps of bias sweeping, and the integration factors can be set. The dynamic IV (or pulse IV) characteristics are good criteria for investigating the current collapse of the devices, which is a very important issue in the GaN-based HEMTs.
Fig. B.2 (a) Configuration of the dynamic IV measurement with a dynamic IV analyzer; (b) the shape of the device for the dynamic IV measurement; (c) the shape of the GSG probe for RF measurements.

2. Capacitance-Voltage (CV) Characterization

Capacitance-Voltage (CV) characterizations are usually conducted on the GaN-based HEMTs wafers via a circular Schottky diode fabricated on them. The configuration of the CV measurement system is shown in Fig. B.3(a), which includes a LCR Meter and a semiconductor parameter analyzer. The LCR meter is used for the measurement of the differential capacitance of the Schottky diode and the semiconductor parameter analyzer is used for controlling the LCR meter, setting measuring parameters, display the CV curves and storing the data. The shape of the Schottky diode is shown in Fig. B.3(b), which is formed by a ring-shape Ohmic contact and a circle-shape Schottky contact in the center.
Fig. B.3 (a) Configuration of the CV measurement with a LCR meter and a semiconductor parameter analyzer; (b) the shape of Schottky diode for the CV measurement.

3. Small-Signal RF Characterization

Basically, the small-signal RF characterization is performed on devices by measuring the scattering parameters (S-parameters) at high frequencies to characterize the RF performances of the device. The configuration of the S-parameters measurements is shown in Fig. B.4, which consists of a two-port vector network analyzer (VNA) and a DC bias source. The measuring system is controlled by a PC running Agilent® IC-CAP software. The bias point and measuring frequencies can all be set via the software.
In order to perform accurate RF characterizations of on-wafer devices, the Impedance Standard Substrate (ISS) is used to calibrate the loss of the coaxial lines loss and to offer the calibrate reference plane to the probe tips. "SOLT" is one of the calibration methods used to measure the "short", "open", "load" and "through" standards. The ISS for SOLT calibration are shown in Fig. B.5.

Fig. B.5 SOLT calibration standards for on-wafer RF small-signal measurement.
With a calibrated VNA, accurate and precise small-signal S-parameter measurements can be easily taken. The S-parameters are the ratio between the reflected and transmitted voltage waves over a broad bandwidth. When applying the sinusoidal small-signals to the terminals of the device, the linear circuit performance is described by its S-parameters.

Apart from its use in the calibration, pad de-embedding is also applied to improve the accuracy of the S-parameter measurements. The simplified pad de-embedding in this work involves an additional S-parameters measurement of the dummy open probe pad, which is similar to the device but without the active region and the gate electrode. The shape of the open pad for de-embedding is shown in Fig. B.6. The inevitable capacitive parasitics associated with the pads can be calibrated, and the reference plane also can be further moved closer to the device plane.

![Fig. B.6 The shape of the “open” pad for device de-embedding.](image)

4. **Large-Signal RF Characterization**

Large-signal RF characterization, or RF power characterization, is different from the small-signal RF characterization, because the device is under non-linear operation for high-power applications. This results in different impedances between
small-signal and large-signal applications. These are important for the optimum design of oscillators, mixers and power amplifiers in RFICs. The large-signal characteristic is sensitive to many factor such as DC bias conditions, frequencies, input and output terminations, signal amplitudes, waveforms and power levels. In order to characterize the device with a large-signal, large-signal characterization is performed with a load-pull system. This system is universally accepted by transistor manufacturers and circuit designers and provides a systematic RF PA design procedure.

To characterize the RF power performance of the device, usually the one-tone large-signal measurement is done with a load-pull system. The configuration of the one-tone large-signal measurement is shown in Fig. B.7, which includes a load-pull system, a DC bias source, a RF signal generator and a power meter. The whole system is controlled by a PC via a software named “Automatic Tuner System” (ATS).

Fig. B.7 Configuration of the large-signal power measurement, including a load-pull system, a signal generator, a DC bias source, and a power meter controlled by a PC.
The load-pull system is utilized for large-signal RF characterization at various tuned impedances, input power levels and bias voltages or currents. Large-signal characteristics, such as power gain and PAE, are easily and accurately obtained with the load-pull system. Before the measurement, calibration is usually done with an ISS “through” pattern.

5. Linearity Characterization

Usually, the linearity characterization of the devices is done by measuring the inter-modulation (IMD) and the adjacent channel power ratio (ACPR).

Linearity characterizations such as high order IMD and ACPR are important so as to characterize the device for any arbitrary system or modulated signals in order to fulfill the system linearity requirements where the output power and efficiency requirements are satisfied. The load-pull system is utilized to characterize the non-linear behavior, such as the third-order input interception point (IIP3), the third-order output interception point (OIP3), IMD and ACPR, of the device under the matched or mismatched situations over a range of power levels. The linearity characterization is basically similar to the power characterization.

Fig. B.8 shows the configuration of the measurement system of two-tone RF large-signal characterization of the device, which is used to characterization the inter-modulation between two RF signals input into the device. The system consists of a load-pull system, two RF signal sources, a DC bias source, a power meter, and a
spectrum analyzer. The whole system is also controlled by a PC with software ATS. The input signal is combined with a power combiner and the output signal is equally split by a power divider for the inputs of the spectrum analyzer and the power meter.

Usually, the third-, fifth-, and seventh-order inter-modulations of the output signal can be measured using this system, and the IIP3 and OIP3 can be calculated from the power sweeping.

![Diagram](image)

Fig. B.8 Configuration of the two-tone large-signal measurement, including a load-pull system, two signal generators, a DC bias source, a power meter, and a spectrum analyzer controlled by a PC.

Fig. B.9 shows the configuration of the measurement system for ACPR characterization, which includes a load-pull system, a RF signal generator which can provide modulated RF signal, a DC bias source, a power meter, and a spectrum analyzer. This configuration is similar to the two-tone measurement expect the input RF signal source, which is a modulated signal here. For some wireless communication systems, such as WCDMA/UMTS, the signal is a modulation signal with a large dynamic range, which has a stringent requirement of the linearity of the
whole system. To characterize the linearity behavior of the system or the components for large-signal operation (such as power amplifier, mixer, oscillator), the adjacent-channel power ratio (ACPR) or the alternate-channel power ratio (AltCPR) is measured. The definition of the ACPR is shown in Fig. B.10, where the signal is a standard WCDMA modulated signal. Similar to the power measurement, before the measurement, calibration is usually done with an ISS “through” pattern.

Fig. B.9 Configuration of the ACPR measurement, including a load-pull system, a signal generator which provides modulated RF signal, a DC bias source, a power meter, and a spectrum analyzer controlled by a PC.

Fig. B.10 The definition of the ACPR, where the signal is a standard WCDMA modulated signal.
6. Noise Characterization

Noise characterization is also important for RFIC design particularly in low noise applications. This characterization reveals the achievable minimum noise figure \( \text{NF}_{\text{min}} \) associated with the device.

To perform the noise characterization on the device, a load-pull system is usually utilized to find out the optimized source impedance \( (Z_{S,\text{opt}}) \) or the optimized reflection coefficient \( \Gamma_{\text{opt}} \) at the desired bias condition and frequency.

Fig. B.11 shows the configuration of the system for noise characterization, which includes a load-pull system, a DC bias source, a noise source, and a noise figure analyzer. By utilizing this system, the minimum noise figure \( \text{NF}_{\text{min}} \) the optimum reflection coefficient \( \Gamma_{\text{opt}} \), the equivalent noise resistance \( R_e \), and the associated gain \( G_{\text{assoc}} \) of the device can be measured. Before the measurement, calibration should be done with an ISS "through" pattern.

![Diagram of noise characterization system](image)

Fig. B.11 Configuration of the noise characterization system, including a load-pull system, a DC bias source, a noise source, and a noise figure analyzer controlled by a PC.
APPENDIX C

THE EXTRACTION OF SMALL-SIGNAL EQUIVALENT CIRCUIT

Fig. C.1 Small-signal equivalent circuit of field effect transistor.

The conventional small-signal equivalent circuit of a field effect transistor (FET) is shown in Fig. A.1. Basically, this equivalent circuit can be divided into two parts:

(i) the intrinsic elements \(g_m, g_d, C_{gs}, C_{gd}, C_{ds}, R_i, \) and \(\tau,\) which are functions of the biasing conditions;

(ii) the extrinsic elements \(L_g, R_g, C_{pg}, L_d, R_s, R_d, C_{pd},\) and \(L_d,\) which are independent of the biasing conditions.

Since the intrinsic part of the equivalent circuit exhibits a \(\pi\) topology, it is convenient to use the admittance \((Y)\) parameters to characterize its electrical properties. These parameters (normalized) are [C-1]:

\[
y_{11} = \frac{R_i C_{gg}^2 \omega^2}{D} + j \omega \left( \frac{C_{gs}}{D} + C_{gd} \right)
\]  

(C.1)
\[ y_{12} = -j \omega C_{gd} \]  
\[ y_{21} = \frac{g_m \exp(-j \omega \tau)}{1 + j R_i C_g \omega} - j \omega C_{gd} \]  
\[ y_{22} = g_d + j \omega (C_{ds} + C_{gd}) \]

with \( D = 1 + \omega^2 C_{gs}^2 R_i^2 \).

For a typical low-noise device, the term \( \omega^2 C_{gs}^2 R_i^2 \) is less than 0.01 at low frequency \( f < 5 \text{ GHz} \) and \( D = 1 \) constitutes a good approximation. In addition, assuming \( \omega \tau \ll 1 \), we have:

\[ y_{11} = R_i C_{gs}^2 \omega^2 + j \omega (C_{gs} + C_{gd}) \]  
\[ y_{12} = -j \omega C_{gd} \]  
\[ y_{21} = g_m - j \omega (C_{gd} + g_m (R_i C_{gs} + \tau)) \]  
\[ y_{22} = g_d + j \omega (C_{ds} + C_{gd}) \]

Expressions (5)-(8) show that the intrinsic small-signal elements can be deduced from the \( Y \) parameters as follows: \( C_{gd} \) from \( y_{12} \), \( C_{gs} \) and \( R_i \) from \( y_{11} \), \( g_m \) and \( \tau \) from \( y_{21} \), and, lastly, \( g_d \) and \( C_{ds} \) from \( y_{22} \). Therefore, the problem is to determine the \( Y \) matrix of the intrinsic device from experimental data. Assuming that all the extrinsic elements are known, this can be carried out using the following procedure (as shown in Fig. C.2):
Fig. C.2 Method for extracting the device intrinsic $Y$ matrix.

- **a)** measurement of the $S$ parameters of the extrinsic device;

- **b)** transformation of the $S$ parameters to impedance ($Z$) parameters and subtraction of $L_g$ and $L_d$ that are series elements;
c) transformations of $Z$ to $Y$ parameters and subtraction of $C_{pg}$ and $C_{pd}$ that are in parallel;

d) transformation of $Y$ to $Z$ parameters and subtraction of $R_s$, $R_s$, $L_s$, $R_d$ that are in series;

e) transformation of $Z$ to $Y$ parameters that correspond to the desired matrix.

By now, we can find, the determination of the intrinsic admittance matrix can be carried out using some simple matrix manipulations if the different extrinsic elements are known. The details of the measurements of the extrinsic elements are described below.

A. Determination of the Parasitic Resistances and Inductances

As Diamant and Laviron suggested, the S-parameters measured at zero drain bias voltage can be used for the evaluation of device parasitics because the equivalent circuit is much simpler [C-2]. Fig. C.3 shows the distributed RC network representing a FET channel under the gate at $V_{ds} = 0$.

![Diagram](image)

Fig. C.3 Sketch of the distributed RC network under the gate electrode yielding equations (C.9), (C.10), and (C.11).
For any gate biasing conditions [C-3], [C-4], the impedance parameters $Z_{ij}$ can be written as

$$z_{11} = R_c / 3 + z_{dy}$$  \hspace{1cm} (C.9)

$$z_{12} = z_{21} = R_c / 2$$  \hspace{1cm} (C.10)

$$z_{22} = R_c$$  \hspace{1cm} (C.11)

where $R_c$ is the channel resistance under the gate and $z_{dy}$ is the equivalent impedance of the Schottky barrier. $z_{dy}$ can be written as

$$z_{dy} = \frac{R_{dy}}{1+j\omega C_y R_{dy}}$$

with

$$R_{dy} = \frac{n k T}{q I_g}$$  \hspace{1cm} (C.12)

where $n$ is the ideality factor, $k$ the Boltzmann constant, $T$ the temperature, $C_y$ the gate capacitance, and $I_g$ the dc gate current.

As the gate current increases, $R_{dy}$ decreases and $C_y$ increases but the exponential behavior of $R_{dy}$ versus $V_{gs}$ is the dominant factor, consequently the term $R_{dy} C_y \omega$ tends to zero for gate current densities close to $5 \times 10^7$-$10^8$ A/m$^2$. In that case, we have

$$z_{dy} = R_{dy} = \frac{n k T}{q I_g}$$  \hspace{1cm} (C.13)

For such a gate current, the capacitive effect of the gate disappears and the $z_{11}$ parameter becomes real:

$$z_{11} = R_c / 3 + \frac{n k T}{q I_g}$$  \hspace{1cm} (C.14)

In addition, the influence of the $C_{pg}$ and $C_{pd}$ parasitic capacitance is negligible and consequently the extrinsic $Z$ parameters are simply determined by adding the parasitic resistances $R_s, R_g, R_d$ and inductances $L_g, L_s, L_d$ to the intrinsic $Z$ parameters.

Then we have
\[ Z_{11} = R_s + R_g + \frac{R_c}{3} + \frac{nKT}{qI_g} + j\omega (L_s + L_g) \]  \hspace{1cm} (C.15)

\[ Z_{12} = Z_{21} = R_s + R_c / 2 + j\omega L_s \]  \hspace{1cm} (C.16)

\[ Z_{22} = R_s + R_d + R_c + j\omega (L_s + L_d) \]  \hspace{1cm} (C.17)

These expressions show that the imaginary part of the Z parameters increases linearly versus frequency while the real part is frequency independent. In addition it must be noted that the real part of \(Z_{11}\) increases as \(1/I_g\).

From the expressions (C.15)-(C.17), the extrinsic elements can be extracted by fitting the real part and imaginary part of the Z parameters. For example, by measuring the gate-current-dependent S parameters of the device (at \(V_{ds} = 0\)) and transform to the Z parameters, the term \(R_g + R_s + R_c / 3\) can be obtained by extrapolating the real part of \(Z_{11}\) versus \(1/I_g\) curve to the point of infinite gate current, as shown in Fig. C.4.

![Fig. C.4 Evolution of the Z_{11} real part as a function of 1/I_g.](image)

Fig. C.4 Evolution of the \(Z_{11}\) real part as a function of \(1/I_g\).
By investigating expressions (C.15)-(C.17), we can find there are four unknown elements in the real part: $R_s$, $R_g$, $R_d$ and $R_c$. To obtain the values, we need an additional relation, which can be:

(i) The value of the sum $R_s + R_d$, which is determined by the conventional method [C-5], [C-6]. It must be emphasized that this determination can be carried out with the network analyzer using the real part of $Z_{22}$.

(ii) The value of $R_g$ if it can be provided from the resistance measurement from pad to pad.

(iii) The value of $R_s$ and $R_d$ provided by dc measurement [C-7].

(iv) The value of $R_c$ if the channel technological parameters are known.

B. Measurement of the $C_{pg}$ and $C_{pd}$ Parasitic Capacitances

To measure the parasitic capacitances $C_{pg}$ and $C_{pd}$, some kind of method named "cold FET" can be employed. As a matter of fact, at zero drain bias and for a gate voltage lower than the pinch-off voltage $V_p$, the intrinsic gate capacitance (i.e., under the gate) cancels, as does the channel conductance. Under these biasing conditions, the FET equivalent circuit is shown in Fig. C.5. In this figure $C_b$ represents the fringing capacitance due to the depleted layer extension at each side of the gate. For frequencies up to a few gigahertz, the resistances and inductances have no influence on the imaginary part of the $Y$ parameters, which can be written as

$$\text{Im}(Y_{11}) = j\omega(C_{pg} + 2C_b) \quad (C.18)$$

$$\text{Im}(Y_{12}) = \text{Im}(Y_{21}) = -j\omega C_b \quad (C.19)$$
\[ \text{Im}(Y_{22}) = j\omega(C_b + C_{pd}) \]  

(C.20)

Thus, the three unknowns \( C_b, C_{pg}, \) and \( C_{pd} \) can be calculated using (C.18)-(C.20).

Fig. C.5 Small-signal equivalent circuit of a FET at zero drain bias voltage and gate voltage lower than the pinchoff voltage.

REFERENCES OF APPENDIX C


APPENDIX D

PUBLICATION LIST

JOURNAL:

[D1] J. Liu, Y. G. Zhou, R. M. Chu, Y. Cai, K. J. Chen, and K. M. Lau, "Highly Linear \(\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{Al}_{0.05}\text{Ga}_{0.95}\text{N}/\text{GaN}\) Composite-Channel HEMTs," *IEEE Electron Device Lett.*, vol. 26, no. 3, pp. 145-147, Mar. 2005.


[D3] Z. Cheng, J. Liu, Y. G. Zhou, Y. Cai, K. J. Chen, and K. M. Lau, "Broadband Microwave Noise Characteristics of High-Linearity Composite-Channel \(\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{Al}_{0.05}\text{Ga}_{0.95}\text{N}/\text{GaN}\) HEMTs," *IEEE Electron Device Lett.*, vol. 26, no. 8, pp. 521-523, Aug. 2005.


CONFERENCE:

[D7] J. Liu, Y. G. Zhou, R. M. Chu, Y. Cai, K. J. Chen, and K. M. Lau, "Al$_{0.3}$Ga$_{0.7}$N/Al$_{0.05}$Ga$_{0.95}$N/GaN Composite-Channel HEMTs with Enhanced Linearity," in Dig. IEDM Tech., pp. 811-814, Dec. 2004.


