Very low BER (down to $10^{-10}$) have been verified using two kinds of emulators prior to silicon implementation: Cadence-Palladium and EVE-ZebuzY. The BER results were later measured on the final application as well.

This chip was built in a 1.2V, 65nm, 7M low-leakage CMOS technology. A total of 91 memory macros (RAM and ROM) occupied nearly 50% (3mm²) of the available IP floor plan area of 6.07mm². Stringent design rules requiring placement of memories in only R0/R180 orientation (uni-directional POLY) and minimum of 80% multi-cut via’s in the design for DFM reasons resulted in a huge challenge in routing such a wire-dominated design.

To reduce the IR drop from an initial 50mV to a final value of 15mV (analysis performed using Synopsys AstroRail), the widths were iteratively modified from a default 4.5µm to 6µm, for metal7 and metal6 in a standard mesh type PG (power-ground) structure.

A selective mix of orthogonal and parallel PG tapping on the memory PG pins across the chip also helped to minimize the IR drop. However this created an additional shortage of routing resources over the memories. Complex data flow between the logic modules and memories further made it difficult for implementation tools to converge on timing and routing together requiring 15 implementation runs for convergence. To counter high routing overflow (~3%), mostly in the vertical direction, a pseudo-hierarchical approach was taken, wherein a set of 4 standard memories in a module were stacked to emulate large memories and signals were routed separately using the non-preferred direction for routing layers with the PG mesh aligned with the top level. Figure 16.3.4 shows the stack of memories, non-default metal5 routing in the vertical direction and the pins of the module that were placed on one side to allow the abutment of these stacked instances to reduce the area since no routing channels were needed now for the routing in between these memory cuts. Eight such sets were instantiated flat at the top level thereby maximizing the routing density over the memory stacks. The use of a 7LM process with the stacked memory concept proved to be just sufficient to address all routing congestion issues when coupled with the routing tool – Magna Blast Fusion.

On-chip variation / NBTI effects, physical net length restrictions for DFM, crosstalk effects and margins added to the complexity of timing closure. Multi-V, low-power methodology was used starting with only HV, (High Threshold Voltage) CMOS standard cells with only incremental replacement/addition of SV, (Standard Threshold Voltage) cells for timing critical paths, a total of just 8% SVT cells were utilized to meet the design’s high performance and low leakage power targets. With PVT conditions (BC 1.3V, 125°C and WC 1.1V, 125°C) a design frequency of 174MHz with timing signoff margins of 50ps Hold and 250ps Setup (Clock Jitter + Power Noise Sensitivity) were achieved. The physical implementation has been performed using STMicroelectronics’ RTL-to-GDS methodology. This integrates a proprietary signal integrity checker with commercial tools that include Magma Design Automation for Physical Implementation and Sierra Design Automation tools for the Floorplan prototyping.

A summary of the chip implementation details and performance is provided in Fig. 16.3.5, while Fig. 16.3.6 shows the chip micrograph.

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References:
Figure 16.3.1: Detail of the LDPC decoder architecture.

Figure 16.3.2: Bit Error Rate comparison versus previously published DVB-S2 decoding algorithms.

Figure 16.3.3: Measured dynamic power consumption of the overall FEC (LDPC+BCH codecs).

Figure 16.3.4: Stack memories with non default direction routing and special power via distribution.

Figure 16.3.5: Summary of the chip implementation details and performance.

Figure 16.3.6: Die micrograph.