Power MOSFET Characterization for Portable Electronics  
(SJK1a-11)  
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**Project overview**

**Introduction**

Every year, billions of electronic devices are produced to meet the market need. It is quite often that a design after fabrication and production is found to be malfunctioning due to the improper design. Failure Analysis is a combination of processes which is used to identify the root causes of the malfunction of a chip. After locating the problems, modification and optimization can be made.

**Aim and Objective**

- Develop a simple fixture design and the procedures for setting up the design for Face Lapping.
- Find out potential stain solution to perform combinational staining so that more feature can be obtained at the same time

**System Block Diagram**

- [Project research](#)  
  - [Samples preparation](#)  
  - [Fixture design](#)  
  - [Staining implementation](#)  
  - [Fixure design implementation](#)  
  - [Images capturing](#)  
  - [Face lapping implementation](#)  
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**Methodology of Face Lapping**

Face lapping is a process removing different layers of an IC chip. The layout of the IC chip can be visualized. Uniformity is the main concern of Face lapping. A stable lapping process is an important factor of obtaining a uniform lapping surface. For this project, a simple fixture design is adopted to achieve a uniform Face Lapping process.

**Proposed Fixture design**

![Simple design of the fixture](#)

Above is the simple design of the fixture. A rigid holder is used as the base of the fixture. The specimen is mounted together with 4 dummy silicon as to stabilize the lapping process.

**Fixure preparation procedures**

1. Heat up the holder and mount the dummy silicon with wax
2. Adjust the thickness of the dummy silicon with abrasive paper
3. Heat up the holder again and mount the specimen
4. Check the tilting of the specimen, remount the specimen if the tilting is too serious

**Factor** | **Solution**
---|---
Holder material | Optical filter glass can be used
Appropriate dummy silicon thickness | 5um thicker than the specimen
Grinding cloth for different layers | Trident cloth for both metal and dielectric layers
Sample tilting | Adjust the dummy silicon thickness accordingly

**Overall result**

M2 layer  
M1 layer  
Poly gate layer  

### Methodology of Cross sectioning

Staining is a general term applied to chemical decoration of device feature, particularly in cross-sectioning. However, it is impossible to obtain different device feature by using only one stain solution.

**Proposed solution**

The problem can be solved by using combinational staining. In this project, six solution is tested. Here are the steps.

1. Using each solution alone to determine whether the solution is acceptable for combinational staining
2. Determine the recipe of mixing according to the result
3. Perform combinational staining and judge the result

**Overall result**

Cross section etch, 20:1 etch and Dash etch is found to be acceptable stain solution to perform combinational staining. The result is judged using the general structure of Trench MOSFET.

**Recipe and Result of combinational staining**

A. 20:1 etch for 5s + Dash etch for 25s
B. Cross section etch for 5s + Dash etch for 25s

![Recipe and Result](#)