OVERVIEW
Designation of the future generation multiprocessor systems is the subject of research in this project. The trend of the latest technology in the field of computing systems is to integrate multiple microprocessors on a single integrated circuit (IC) chip and to build also high-speed optical waveguide networks among them to enhance the speed of the calculations. This technology, with its merits of being small yet fast, could be expected to bring the performance of today’s supercomputers into laptops or even smaller devices like mobile phones in the future.

BACKGROUND
A hybrid microchip architecture combining electronic and optical interconnection takes advantage of the high performance yet keeps the cost low. One typical example of such topology is named 2D Augmented Folded Torus Network (Fig.1), designed by Lightwave Research Lab from Columbia University [1]. Along with studying the designation of this topology I built a simulation platform analyzing the relationship between throughput of the networks-on-chip (NoCs) over parameters including clock cycle and size of the network. A comparison with regular 2D torus network (Fig.2) was also illustrated.

Simulations were performed with different network sizes from 2*2 to 6*6, and clock cycles ranging from 80ns to 50000ns. Y-axis represents the throughput per unit time.

SOFTWARE IMPLEMENTATION
Hardware description language system C is used. It is basically C++ with extra class libraries for convenience of describing hardware behaviors including ports and signals. Four types of switches are inherited from a generally designed router for sake of code reuse. A total number of 256 ports are required for each switch together with corresponding signal connections.

LIMITATIONS AND CONCLUSION
Some of the functionalities of the hardware design are not implemented in the simulation platform due to unfeasibility or limitation of resource.

1. Address encapsulation: a new indexing system is applied instead.
2. Path multiplicity: due to limitation in stack size, only single path is implemented.
3. Limited size of the network.
Based on the simulation result, it is concluded that the described folded torus 2D network is not as well performing as a simple and regular 2D torus network in terms of throughput.