Optical and Electronic Network-on-Chip for Multiprocessor Systems

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As technology advances, more and more processing cores are included on one chip. The effective communication between cores has become one of the most challenging issues. One of the most feasible solutions to tackle this problem is to introduce optical network into the chip and cooperate with the currently existing electronic network. The objective of this project is to design a fast and scalable centralized controller for an optical network.

Introduction

The centralized control unit proposed in this project is based on optical turn-around routers (OTAR). It applies Deterministic Central Control Protocol on a fat tree based optical network-on-chip (FONoC). The performance data of the control unit is gathered by a synthesis tool and is evaluated with different network sizes. This project designed a centralized control unit and evaluated the speed, power consumption, area cost and scalability.

Methodology

The deterministic central control protocol divides the routing process into four steps. I therefore divide my design into four parts strictly related to the four steps of the protocol. The parallelism is maximized for all four steps to achieve the lowest delay. The four steps are run in pipeline and the bottleneck would fall to the slowest step. The routing is done by hardware and the synthesis of the hardware is done by Design Compiler. The simulation and testing is done by PSPICE which is embedded in ORCAD.

Implementation

The design is implemented by VHDL. The four steps of the deterministic central control protocol are path finding, check links, solve collision and update links. Step one is to calculate the deterministic path for each request. Step two check all the required links with the current link information and see if there is conflict. Step three resolves the interdependence between path requests and step four configures routers and update link status.

Evaluation

I have conducted the synthesis for four, eight and sixteen processors. Each step in the deterministic central control protocol is synthesized separately and the results of synthesis are gathered. The result that I obtained shows that the throughput of the centralized control unit does not increase linearly. The rate of increase decreases exponentially. On the other hand the area cost and the power consumption of the centralized control unit increased dramatically. The increase is around the square of the increase of the number of processor.

Conclusion

Although the area cost and power consumption of a centralized control unit are very low when the number of processors is low, the area and power consumption increase approximately in a square ratio with the number of processors in the optical network. This may cost big trouble for large networks.