Interconnect Layer Thermal Modeling and Its Applications for 3-D Integrated Circuits

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Project Overview

Three-Dimensional Integrated Circuits (3-D ICs) based on layer-stacked and wafer-bonding technique is a popular method to further enhance the integration scale as well as to reduce the on-chip interconnection cost.

However, 3-D ICs’ extremely high power density and thus high on-chip temperature are critical issues to maintain proper functions.

So our project mainly targets on:

- A thermal model for 3-D IC architecture-level thermal simulation
- Potential applications for our thermal model

Motivation

The package of 3-D chip makes the modeling of interconnect layer important for the following reasons:

1. High conductivity contrast between materials
2. Complex interconnection structure

Modeling Methodology

Our simulation shows that the conductivity is highly related to the metal density, especially via density. So we use an empirical equation to fit for the relationship between density and relative conductivity.

As we can see from the figure, via density and conductivity conforms an exponential-like relationship.

![Graph showing exponential-like relationship between density and conductivity]

So we use the following equations for the fitting:

\[ \delta = 1 + d \left( -e^{-\frac{d}{d_0}} \right) \]

Where

\[ d = \sum \frac{V_i}{S_i} \]

We use benchmarks to get sample points for the fitting.

Result

We use our fitting function to do the simulation. We also use methods from others’ work as reference. The result is shown in the figure:

![Simulation results showing fit and comparison]

Conclusion

- In our project, we propose a interconnect layer model for 3-D IC thermal simulation.
- We use an empirical method to characterize the relationship between metal density and thermal conductivity.

Our model can achieve results with average error less than one degree.