Abstract
This project is mainly focused on the testing of the avalanche capability of the on wafer Power MOSFET using the Unclamped Inductive Switching (UIS) test circuit. At the beginning of the project, background information study will be taken place as it provides general information about the Power MOSFET. The UIS test circuit and its failure modes will also be studied. The next step is the simulation of UIS circuit. This will be based on the background information, such as simulation device modeling and so on. The simulation circuit will be used to verify the theoretical operation of the UIS circuit. The final stage of this project is to build an UIS test circuit. The experiment is focused on the on wafer Power MOSFET devices and the Current Failure mode.

Aim and Objective
The first objective of the project is to understand the Power MOSFET. Background information studying provides intuition about variables that are involved in this project. Based on the understanding, the avalanche capability of Power MOSFET will be focused. This is an important parameter for device’s design in the past twenty years. Since the size of the Power MOSFET is significantly reduced, the avalanche behavior becomes sensitive during high voltage switching. The Avalanche capability is recently regarded as an indicator to differentiate the performance of Power MOSFET devices. To evaluate this parameter, a testing circuit is necessary as it could estimate the tolerance of the breakdown during high current inductive switching. Thus, the second objective of this project is to build a circuit to test the avalanche capability of the on wafer devices. As this project covers a wide range of topics such as devices characterization, circuit design and devices analysis, it provides all round understanding in these topics.

Methodology
The Power MOSFET is placed in the center of the circuit, called device under testing (DUT). The gate of the Power MOSFET is connected to the resistor R1 and the pulse generator. The drain of the Power MOSFET is connected to inductors L1, resistor R2 and also to the Power Supply. In order to start the test, the Power Supply will be turned on and it will generate a DC voltage to the drain of the power MOSFET. The pulse generator will also be switched on in order to turn on the Power MOSFET. After a period of time, the pulse generator will stop providing voltage to the gate. There is a rapid increase of voltage at the source to drain (Vds) of the DUT as the inductor is discharged, because no energy can be stored in the inductor. This voltage could be observed from the oscilloscope. The current probe is used to detect the magnitude of the current. The current probe is connected to the oscilloscope so that it can convert the pulse to waveform.

UIS Circuit Simulation

Mathematical formula

Summary of Simulation

Conclusion
Portable devices play a major role in modern society. People nowadays rely on their portable devices to communicate, obtain information, etc. Therefore, testing the fundamental units of the portable device such as the Power MOSFET will be useful to push the power limitation further and hence, improve the quality of the portable devices. The objective of the project is achieved as the Unclamped Inductive Switching (UIS) test circuit is built. The building of the test circuit is based on the background information study of the Power MOSFET and UIS failure and also simulation. The test circuit is used to measure the avalanche capability of the Power MOSFET. And the waveform of the breakdown current and voltage in the Current Failure Mode is also obtained from the UIS experiment stage. Since this project covers a wide range of topics, it is a valuable for us to have this experience.

Discussion
It is observed that the current is increasing when a larger pulse was applied. From Figure 5.15, if the pulse duration is larger than or equal to 2.0 μs, the devices will be in the current failure mode. From Figure 5.14, it could be discovered that the device could sustain up to 3.4 divisions times 0.5 A = 1.7 A. The breakdown voltage is around 72 Volts and the avalanche energy is (152) = 72V x 1.7A x 4.4μs x 1.344×10J. The conclusion of the simulation results is that the simulated waveform is exactly the same as the experimental result. When the power dissipation increases, the energy from the inductor will charge the device and the breakdown will occur.

Experiment Results

Vth = 5.3V ± 0.2V, When the voltage of the device is less than 100mV in the test circuit. The device is said to be failed to satisfy this condition, since it is the standard value of UIS measurement under that failure mode. The device used in the measurement is 0.02mm2, and the maximum current before the breakdown of the device is 1.7A. From this data, the current density could be calculated by 1.702A/cm2.