Project Overview
Analog and Digital Converter (ADC) is widely used in the daily life. Among of these ADCs, Sigma Delta ADC (SDADC) is the highest resolution one. The performance of SDADC relies on the oversampling ratio and the compensated system design.
In our project, we would design a 18-bit Low Power Continuous time SDADC. By implementation as CT, it can obtain high resolution but without consume too much power and contains an anti-aliasing function with better a noise reduction result.

Methodology

![Block Diagram of SDADC](image)

The block diagram shows the structure of the discrete time SDADC.

Design Phase
Firstly, we are looking for more than 18 bit resolution SDADC in a noiseless simulation system. After the system is performed, the addition noise would be inserted into the system. Observe the maximum noise margin in order to achieve 18 bit. Also, apply DT to CT transformation to get a CT SD modulator. Finally, System model in CT SDADC as shown below.

Right hand side shows the spectrum of 18-bit SDADC. The 10kHz component is the signal and we can notice the noise is shaping to high frequency.

Circuit Implementation by gm-cell

![Schematic of SD Modulator](image)

The Schematic of the SD modulator:

Conclusion
The SNR can achieve at least 18 bits resolution in system modelling. However, we only get about 18bit in circuit. We find that it is quite difficult to implement in circuit level. Because of the small value point, current mismatch error is larger lead to larger non-linearity error in gm cell. Also, the common mode gain cannot suppress too low. As a result, the dc offset level is larger. We would minimise the above drawback in future.