Introduction

ApplTech Limited is aables to develop high-performance, high-reliability and cost-effective system-on-chip devices. MCUs are the company's primary products. In general, MCUs do not implement any external address or data bus since they support memory operations on the same chip with CPU. Therefore, an analog-to-digital converter (ADC) is required. A dual-slope ADC, which is known as its simple structure, moderate to high resolution and low power, is adopted in the project.

System Block Diagram

The dual-slope ADC includes a pre-amplifier, a buffer, a multiplexer, an integrator, and a comparator. The preamplifier circuit includes a differential and a single-ended amplifier. The amplifier adopts chopper stabilization techniques to eliminate the offset. The integrator circuit is an auto-zero switched capacitor design that minimizes the error in the charging and discharging phases. A latched comparator is coupled with the integrator to offer precise and accurate comparison. The comparator uses three pre-amplification stages to improve the speed of the conversion.

Pre-Amplifier Stage

Chopping DTS Amplifier

The main body of the present DTS amplifier adopts a folded cascode structure with PMOS input stages. A source follower is appended as a buffer to drive the low-pass filter in the latter stage. A pair of chopper switches is embedded right after the input. The second pair of chopper is installed before the output stage. This chopping technique improves the accuracy of the first stage in the system significantly.

Integrator Stage

Auto-Zeroing Amplifier

A switched-capacitor auto-zeroing amplifier is designed for the integrator stages. It consists of seven switches and one offset capacitor. This structure needs an extra phase for auto-zeroing process. The amplifier has to be disconnected from the signal path during phase one in order to sample and hold the offset and noise. Hence, during the normal integration, the offset would be compensated by the offset capacitor.

Comparator Stage

Latched Comparator

A latched comparator is introduced in the present project. A traditional single op-amp comparator needs to be designed with an ultra-high gain to obtain a fast response time. Thus, the comparator would consume large power. A latched comparator takes the advantage of a regeneration phase to accelerate the speed to pull up or down the output. It thus requires less power and provides faster comparison.

Project Implementation

Project Result

Overall Performance:

Supply voltages: 2.5V
Production technology: TSMC 0.35μ
Resolution: 12-bit
Sampling rate: 10 samples per second
Power consumption: ≤ 100μW
Input differential signal range: 0.1V

Comparison: Proposed: Achieved

Amplitude Set: 0V
Three differential input signals: 5mV, 10mV, 15mV
Input: 1.0V
Input frequency: 10Hz
Comparator: Digital inputs 5mV
Comparator: Digital inputs 0.5mV