SJK2b-06 Packaged and Wafer Level
Semiconductor Failure Analysis

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OVERVIEW

1. Introduction

Nowadays, huge amount of Integrated Circuit (IC) are fabricated to fit the electronic market. However, some of them may not function properly due to the problem occurred in fabrication process or in design phase. To find out the root problem of the IC, Failure Analysis (FA) is a key concept to solve these problems. Due to the life time of the electronic product are becoming shorter and shorter, the time for FA should be minimized.

In FA, Reverse Engineering and Optical test for an IC required a full picture of IC that has a high resolution. Therefore, by speed up this process, the efficiency of the FA can be improved.

2. Aims and Objectives

- To develop an algorithm to merge the fragmented image automatically.
- To optimize this algorithm.
IMPLEMENTATION

**Acquire Image**

An IC was put on the stage of Confocal Microscopic, then, by changing the xy position to picture all the parts of the IC and save as JPEG format. Only x or y position can be changed each time to make sure all the neighboring image have either same x coordinate or y coordinate.

**Loading Image**

The images will be loaded to software called MATLAB. For each pixel, it contains 3 values for Red, Green and Blue. Each value ranged from 0 to 255 and combination of them can form the original color of the picture.

**Positioning**

Two neighboring images will be tested to find the suitable position that the image should be merged.

**Merging**

Merged two image according to the suitable position found.
RESULT

23 images merged by using IM1000, time used: 9 minutes and 1 second.

23 images merged manually, time used: 15 minutes and 20 seconds.

23 images merged by using new algorithm and MATLAB, time used: 16 minutes and 6 seconds.