Introduction

Testing constitutes a very important task in the Integrated Circuit design flow chart. Chip testing and debugging can be very time consuming and costly. Nowadays, different chip testers appear in the market for checking the malfunction of chips. They are either:

- Huge in size and expensive (may cost up to $1 million US!)
- Complicated and hard to use
- Small and for limited models only
- Do not provide useful test results and information

Aims and Objectives

In this project, we aim to develop a low-cost, portable tester with a user-friendly interface enabling users to handle the testing procedures easily.

The tester is based on the Field Programmable Gate Array (FPGA) platform, a personal computer and a Device Under Test (DUT) board, to perform different tests on digital chips.

Features of Our Product (40-pin Universal Tester):

1. Functional Test
2. Power Dissipation Test
3. External Signal/Clock Input
4. Waveform-based Display
5. Large Test Case Size (up to 1 million)
6. Rapid Test Cycle Time (up to 0.5 us)
Methodology

1. System Diagram

2. Functional Test

Stage 1 – Capture Testing Data
The user input the test data in GUI which will be sent to the FPGA and stored.

Stage 2 – Drive Signals to the Chip
The FPGA sends the input signals to the chip, and collects output signals from this later.

Stage 3 – Result Analysis
The FPGA compares the collected outputs with the expected ones. If they match, then the chip is functionally correct.

Stage 4 – Display Results to User
The compared results are sent to the PC and displayed in GUI.

3. Power Dissipation Test

Significance
With this function, the user can measure the power required by the chip to function.

Procedure
In the DUT board, the user can connect an ammeter to the headers in serial, and calculate the power by measuring the current and the voltage.
4. Voltage Selector & External Signal/Clock Input

**Significance**

Different digital chips, especially the microprocessors and controllers, may require clock inputs with different cycles. For each pin, the user can provide input signals in different voltage level (3 – 15V) or an external clock to the chip.

**Results**

Our tester can perform testing on different types of chips, including:

- **Arithmetic and Logic Units**
- **Sequential Logics**
- **Buffer and Binary Counters**
- **Multiplexers and Decoders**
- **Logic Building Blocks**
- **Simple Logic Gates**

It supports up to 1 million test cycles with a period of about 500 ns.

**Testing Speed**

![Graphical User Interface]

The signal output from the FPGA is distorted significantly when the test cycle time is less than 0.2 us.

**I/O Performance**

Future work will be dedicated to improving the speed and providing analog interfaces.