HIGH DEFINITION PROJECTION DISPLAY

HH2b-05

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**PROJECT OVERVIEW**

High-definition television (HDTV) allows broadcast of television signals with a higher resolution than traditional formats (NTSC, SECAM, PAL).

Nowadays, the HDTV projector has become popular in many organizations due to its high resolution which produces high quality images. In the US, there are different HDTV channels broadcasting. Therefore, it is a trend that HDTV broadcast channels will soon be developed in HK. As HDTV will be popular, it is worth building an HDTV projector.

This project will focus on building an HDTV projector which can accept multiple input signals (Component-YPbPr, PC-VGA, Composite and S-Video), providing double frame rate images to prevent image flickering with output image resolution of 1280×768 pixels.

HDTV Micro-display Driver Board (Top Layer)  
HDTV Micro-display Driver Board (Bottom Layer)
DOUBLE FRAME RATE TECHNIQUE

To double the frame rate, two sets of SDRAMs (SDRAM_A, SDRAM_B) are required. Input data was written into SDRAM_A while the data stored in SDRAM_B will be read out twice at the same time.

Timing Relationship between Write and Read Procedure
**Signals Output From EL8658**

The resolution of the outputs was 1280×768. The expected frequency of the output Vsync, Hsync and Dataclk should be 60Hz, 48.2kHz and 80MHz respectively. The following figures show the result of the signals measured by CRO.

Output Signals from EL8658 (Dataclk, Vsync)

Output Signals from EL8658 (Hsync, Vsync)

**Signals Output From Spartan IIE S50E**

At the end of the first frame and at the beginning of the second frame, DISP is in logic low which mean there is no useful data in this period.

To have a clear image, the signal SCLK needed to be set to logic high within the DISP period.

Relationship between the Signal DISP and FRAME

Relationship between the Signal SCLK and DISP