High Definition Projection Display
HH1-04

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In this project, the projector can support a DVI input from the PC interface. The input signals from the DVI are first input to the Silicon Image SiI151A and then the resultant digital signals will be input to the FPGA Xilinx Spartan IIE S50E.

Several features have been added to this projector so that the quality of the output images is greatly improved. These features includes bit differing, bit flipping and double frame rate.

The projector can support two input resolutions which are $1280 \times 1024$ and $1024 \times 768$. The frequency of the input of both resolutions is 60 Hz. After a series of signal processing, the output images are projected on a panel of resolution $1280 \times 768$ at 120 Hz. In this process, pixels data is stored temporarily in the SDRAM chips in our driver board.
The driver board is composed of four layers. Most of the routings were placed on the top and bottom layers. One of the middle layers is for ground shielding and the other one is for other routing purposes such as 3.3V and 1.8V supply voltage.

In this figure, the blanking time constraints between the HSYNC and data enable can be visualized. The access of data in correct timing is carried out in the FPGA.
Simulation results

The simulation results are obtained from the project navigator and the model simulator. The simulated results are very important for us in order to predict the expected waveforms in our design phase.

Results

Figure 7: Bit Differing
Because of the loss of the last two bits of pixel data, bit differing is applied to have a more accurate color sampling. Since each frame will be projected twice in each cycle, the image of the first frame compensates the color loss by this technique, where the 2\(^{nd}\) LSB is added to the 3\(^{rd}\) LSB, so the average color of two frames will be closer to the original color.

Figure 8: Projected Images
Images are projected successfully on the panel with double frame rate and bit differing.