Transceiver IC Design for Home Network System

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Introduction
More and more electronic devices are used in a home network system today. For the communication between the devices, transceiver IC is needed to handle the signal transmission. The signals are often coded before the transmission. Manchester Code is one of the coding formats always used. For digital communication, CMOS technology is always used to design the transceiver IC.

CMOS
CMOS is the short term of complementary metal-oxide-semiconductor. Basically, this transistor acts as a switch to construct the logic. For example, when the switch is open, it represents ‘0’. When the switch is closed, it represents ‘1’. It can be used to construct more complex logic circuit.

Manchester Code
Manchester encoding is a synchronous clock encoding technique which represents a logic ‘1’ bit as a 0 to 1 transition and a logic ‘0’ bit as a 1 to 0 transitions as shown in Figure 1

Aim
Our aim is to design a receiver IC to decode the received signals in Manchester Code based on CMOS technology.

Computer-Aided Software: CADENCE
It is a software which provides a platform to design the circuit schematics and the layouts of the IC. It also helps to do simulations of the circuit to ensure the circuit has the proper function and examine the performance.
Methodology

Approach:
The Manchester decoder can decode the encoded data with a reference clock with 5-12 multiple of frequency of the input signal. The Phase Locked Loop (PLL) is used to find out the clock of the input signal and output a clock around 5-12 multiple of frequency of the signal. While the output clock is input to the decoder, the signal can be decoded.

Phase Locked Loop (PLL) Circuit
Function: clock recovery

Input: the Manchester signal
Output: the clock with 5-12 multiple frequency of the input signal

Manchester Decoder
Function: decode the Manchester Coded signal

Input1: Manchester Code signal
Input2: a reference clock provided by the Phase Locked Loop (PPL) circuit
Output: decoded signal in NRZ format (‘0’ represented by low voltage level, ‘1’ represented by high voltage level)
Simulation Result

Phase Locked Loop circuit

The output clock is locked at about 220ns and it is within 5-12 multiple of frequency of the input signal.

Manchester Code Decoder

The signal input is ‘1 0 0 1 1 0 1 1’ with a frequency 166.667M Hz while the frequency of the clock REC_CLOCK is around 1333.333 M HZ (8 times input clock rate). The DATA_OUT shows that the decoder signal is ‘1 0 0 1 1 0 1 1’ in NRZ format.