Standard Cell Library of AMI 0.35µm CMOS Technology and Automatic placement and routing for CMOS imager

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Overview

The aim of the project was, via the development of a standard cell library, to build the digital control circuitry for a CMOS imager. The control circuitry was realized using automatic placement technology. This shortens the design time of a CMOS imager and makes the product cheaper. With an increased number of transistors being implemented on a single chip, the design time increases and so does the cost of the product. Designing the control circuitry of a complex digital circuitry using automatic and placement and routing tools reduces the cost making the CMOS imager suitable for low cost consumer electronic application.

Standard Cell Library Design

A total of 61 commonly used gates were constructed based on 0.35 \( \mu \) m technology. The library includes 42 standard gates, 7 composed AOI, OAI gates, arithmetic operators, buffers, latch and Flip-flop, and other edges and filler cells. After considering the floor-planning of the cells, optimizations were performed, and the output performances of the cells were extracted into a data sheet. An example of the data extracted for each cell is shown in the following example.
Design automation of control circuit of the CMOS imager

The digital control parts of CMOS imager, which includes the electronic shutter, row and column decoders, were designed by first building the behavioral models. This was followed by performing synthesis via which the gate level description of the control circuit was obtained. By performing the logic optimization, we further optimized the design. Finally, the layout of the design was obtained using automatic placement and routing.
Conclusion

We demonstrated that use of standard cell library in speeding up the process of designing the control circuit of the CMOS imager. This is very important in order to design a low cost CMOS camera. The designed standard cell library can, in fact, be used in any digital circuit.