Title: Senior Processor Development Engineer, Hong Kong

In May 2008, HiSilicon-Huawei setup an R&D center in Hong Kong, focusing on communication chipset development. Today, we are expanding our R&D work to processor core development. The core would be used in a wide range of ASIC for different Huawei products. We are looking for enthusiastic and high caliber engineers at all levels to join our team, to support the development from system and architectural design, modeling and benchmarking, micro-architecture design to front-end implementations and verifications.

The Senior Processor Development Engineers will be responsible or take part in defining the micro-architecture of different major functional units of a processor core, including but not limited to the instruction fetch and dispatch unit, execution unit and the ALU, load store unit, memory management unit, and building blocks for different level of caches. The individual shall be responsible or contribute to the various phase of the development work, including but not limited to feasibility studies, cost and power estimation, performance and functional modeling, software benchmarking, micro-architecture definition, front end design and verification, and synthesis. The individual shall work closely with the chief architect and the team to deliver the processor core that meets the requirements of high performance, low power, and scalability for data plane networking application.

Responsibilities

✓ Interact with the Chief architect and SoC architect, software teams and ASIC product development teams to define the micro-architecture of the Multi-thread Processor core including memory hierarchy and various interconnects
✓ Evaluate and perform trade off analysis of hardware implementation between performance, cost and power.
✓ Define verification and validation strategies at different levels for the processor core and carry out the related work to ensure functional correctness.

Desired Skills and Experience

✓ Minimum of 10 years of proven design or verification experience in complex processor projects
✓ Experience with Multi-Core, multi-threaded processors architecture/design/verification
✓ Experience with designs of complex high speed RTL modules, or Experience with constrained random and formal verification
✓ Experience with the design/verification in one or more of the following disciplines
  ■ Multi-level cache hierarchy
  ■ multi-core/multi-thread system
  ■ instruction fetch and dispatch unit
  ■ Load Store Unit
  ■ Execution, Integer and Floating Point Unit
  ■ Memory Management Unit
  ■ Interrupts and Exception Handling
  ■ Processor Core Virtualization
✓ Good understanding of computer system architecture, memory systems or cache coherency
✓ Good understanding of ARM instruction set
✓ Good understanding high speed circuit and low power design is a plus
✓ Good understanding of TCP/IP networking/service packet protocols is a plus
✓ Must be a highly organized, detail-oriented self-starter, who works well independently, as well as in a team environment
✓ BS or higher degree in Electrical/Computer Engineering with experience in ASIC design/verification.
✓ Good verbal and written communication skills
✓ Candidates with less experience will be considered as Processor Development Engineer

Contact: matthew.leung@huawei.com or lo.wing.yee@huawei.com