Title: Senior ASIC Design Engineer, Hong Kong

In May 2008, HiSilicon-Huawei setup an R&D center in Hong Kong, focusing on communication chipset development. Today, we are expanding our R&D work to next generation products that would be used in a wide range of Huawei products. We are looking for enthusiastic and high caliber engineers at all levels to join our team, to support the development from system and architectural design, modeling, micro-architecture design to front-end implementations and verification.

The Senior ASIC Design Engineers will be responsible or take part in defining the micro-architecture of different major functional units of a communication system, focusing on the MAC and physical layer. The individual shall be responsible or contribute to the various phase of the development work, including but not limited to feasibility studies, cost and power estimation, performance and functional modeling, micro-architecture definition, front end design and verification, and synthesis. The individual shall work closely with the rest of the team to deliver the communication SOC that meets the requirements of low cost, low-power, and high performance for wireline networking application.

Responsibilities
✓ Perform architecture, micro-architecture and logic design using synthesis tools for SOC product.
✓ Verify design by computer simulation and/ or emulation.
✓ Prepare and maintain block diagram, schematics and components information.
✓ Oversee and perform layout design, timing analysis and ECO logic changes.
✓ Evaluate and characterize FPGA/ASIC prototype units.

Desired Skills and Experience
✓ Minimum of 5 years of proven design or verification experience in complex SOC projects
✓ Experience with communication ASIC architecture/design/verification
✓ Experience with the design/verification in one or more of the following disciplines
  ▪ DSP Algorithms, e.g. Digital Filters, FFT etc.
  ▪ Forward error correction Algorithm, e.g. LDPC, Reed Solomon, Trellis Coding, Viterbi etc.
  ▪ Noise Cancellation Algorithms/Scheme, e.g. Interleaving, Echo Cancellation, MIMO, etc.
  ▪ Network and High Speed Interfaces, e.g. XGMII, RGMII, GMII, SERDES
  ▪ SOC processor and peripherals, e.g. ARM cores, DSP cores, SPI, UART, GPIO etc.
  ▪ TCP/IP networking/service packet protocols
✓ Knowledge of simulation and synthesis tools on FPGA/ASIC
✓ Must be a highly organized, detail-oriented self-starter, who works well independently, as well as in a team environment
✓ BS or higher degree in Electrical/Computer Engineering.
✓ Good verbal and written communication skills
✓ Candidates with less experience will be considered as ASIC Design Engineer.

Contact: eric.ng@huawei.com